Cisco Support Community

Expert Series Webcast

CRS-3 Architecture

Thiago Duarte Lopes

High Touch Technical Support – HTTS
CCIE R&S | SP #45415
Feb 24, 2016

Expert Series Webcast ao vivo

CRS-3 Architecture

Thiago Duarte Lopes é engenheiro de suporte a clientes do Time de HTTS (High Touch Technical Support) onde atende a clientes premium da Cisco em toda América Latina. Em outubro de 2010, Thiago se juntou a Cisco como engenheiro on-site para o cliente CLARO BR passando posteriormente para o time de engenheiros do TAC, tendo suportado as filas de Segurança e Routing & Switching. Antes da Cisco, Thiago começou sua carreira na área de transmissão via satélite tendo atuado como engenheiro em empresas como Embratel (Star One), Oi e Hispamar Satélites. Formado pelo Centro Federal de Educação Tecnológica Celso Suckow da Fonseca (CEFET/RJ) em Técnico Eletrônico assim como Engenheiro Elétrico com ênfase em Eletrônica e é fluente em Português, Inglês e Espanhol. Possui as seguintes certificações Cisco: 2x CCIE R&S | SP, CCNP R&S, CCNP Security, CCIP, CCNA R&S, CCNA Security, CCNA Wireless e CCAI.

Thiago Lopes

Tema: CRS-3 Architecture

Participação do especialista

Gregório Bueno

Engenheiro de Suporte ao Cliente TAC

Obrigado por estar com a gente hoje!

Durante a apresentação, serão feitas algumas perguntas para o público.
Dê suas respostas, participe!

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Envie a sua pergunta agora!

Use o painel de perguntas e respostas (P&R) para enviar suas perguntas, os especialistas irão responder em tempo real.

CRS-3 Architecture

Webcast Comunidade de Suporte Cisco em Português

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Webcast
CRS-3 Architecture

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Feb, 24th 2016

AGENDA

- CRS-3 Architecture
- CRS-3 Life of a Packet
- CRS-3 Troubleshooting Commands

Cisco CRS-3 Routing System - Overview

CRS-3

- 3.5x Capacity Upgrade
  - From 40G/Slot to 140G/Slot in existing chassis, same power profile
  - In-service upgrade in all form-factors for operational ease
  - Dense 10GE, Standards-based 100GE modules
- Video Leadership
  - Built-in hardware video monitoring for rich experiences
- Superior 100GE Implementation
  - Single flow at Layer 3 (not 2x50)
  - Fully redundant config (no active-active fabric need)

CRS-3 Multishelf Systems

Switch Fabric

- Fiber cables are used to interconnect LCC through SFC
- Interchassis management system control plane traffic does not pass through fiber cables

CRS
16-slots Linecard Chassis

CRS-3 16-slot Line Card Chassis

- Midplane design with front & rear access
  - ➢ Front
    - 16 PLIM slots
    - 2 RP slots + 2 Fan Controllers
  - ➢ Back
    - 16 MSC Slots
    - 8 Fabric cards
- Dimensions:
  - 23.6” W x 41*” D x 84” H
  - 60 W x 104.2 D x 213.36H (cm)
- Power: ~13.2 KW (AC or DC)
- Weight: ~1600 lbs/723kg
- Heat Dis.: 41000 BTUs

Q&A

Pergunta 1: É possível inserirmos uma MSC-40 em um chassis enhanced?

(a) Sim

(b) Não

CRS-3 16-slot Line Card Chassis

- The CRS-3 system is completely compatible with existing and future components of the Cisco CRS Family. It reuses existing Cisco CRS-1 components such as the chassis, power, fan trays, and fiber interconnects. It is also compatible with Cisco CRS-1 components such as route processors and all 40-Gbps line cards.
- Compatible with all current Cisco CRS-3 Family modular services cards (MSC), forwarding processors, interface modules (PLIM), route processors, and fabric cards.
- Compatible with all current Cisco CRS-1 Family modular services cards (MSC), interface modules (PLIM), and route processors.

CRS-3 16-slot Line Card Chassis Components (CRS-16-LCC)

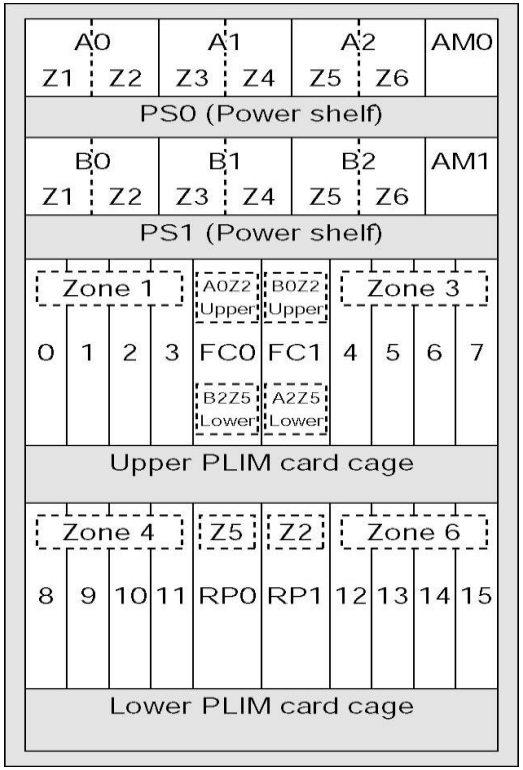
- Two route processors
  - 16-Slot Route Processor (CRS-16-RP)
  - 16-slot Route Processor, revision B (CRS-16-RP-B)
  - 16 Slots 6 Gb Performance Route Processor (CRS-16-PRP-6G)
  - 16 Slots 12 Gb Performance Route Processor (CRS-16-PRP-12G)
- Two Cisco CRS-1 16 slot system fan controllers (CRS-16-LCC-FAN-CT)
- Eight Cisco CRS-3 16 slot system fabric cards (CRS-16-FC140/S)
- Two power shelves (either DC, AC type Wye, or AC type Delta) or Modular
  - AC Delta Power Shelf for 16-Slot LCC (CRS-16-LCC-PS-ACD)
  - AC Wye Power Shelf for 16-Slot LCC (CRS-16-LCC-PS-ACW)
  - DC Power Shelf for 16-Slot LCC (DC Power Shelf for 16-Slot LC)
- Two alarm cards (CRS-16-ALARM)
- Two fan trays (CRS-16-LCC-FAN-TR)
- One fan filter

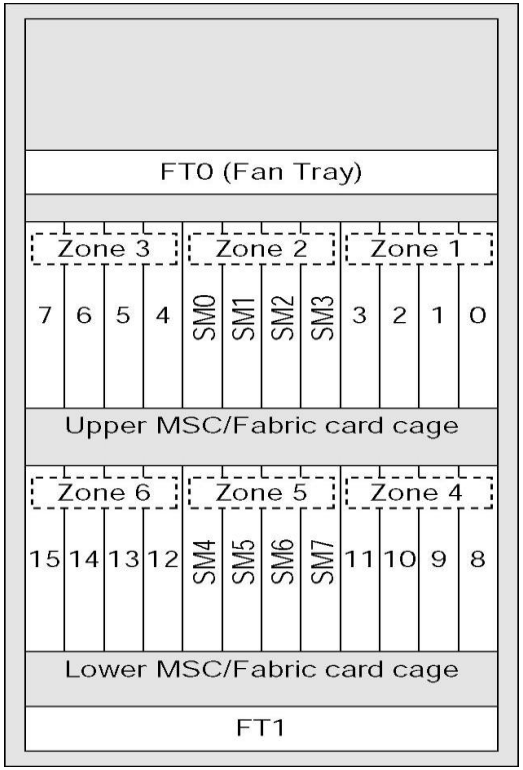
CRS 16-slot Enhanced Chassis (CRS-16-LCC-B)

The CRS 16-slot linecard chassis was redesigned and released in 2011 as CRS-16-LCC-B. The following changes were made:

- The midplane on the Cisco CRS 16-Slot Line Card Chassis Enhanced router is redesigned to support 400G per slot (future fabric replacement => CRS-X).
- A new reduced height Power Shelf has been introduced for the Cisco CRS 16-Slot Line Card Chassis Enhanced router, which results in larger space for air intake (at the bottom of the chassis). This increases the overall cooling efficiency of the chassis.
- A new Alarm Card has been introduced for the Cisco CRS 16-Slot Line Card Chassis Enhanced router that is designed to fit in the new reduced height Power Shelf.
- The Cisco CRS 16-Slot Line Card Chassis Enhanced router Fan Controller monitors and controls nine cooling fans per fan tray using Pulse Width Modulation (PWM).
- The Cisco CRS 16-Slot Line Card Chassis Enhanced router removes the zone circuit breaker and power-zoning requirement.
- The Legacy power shelves, alarm modules, fan trays and fan controllers are not supported with the 16-Slot Enhanced Chassis (CRS-16-LCC-B).

CRS-3: 16 Slot Line Card Chassis Slot Numbering





Fixed Power Architecture

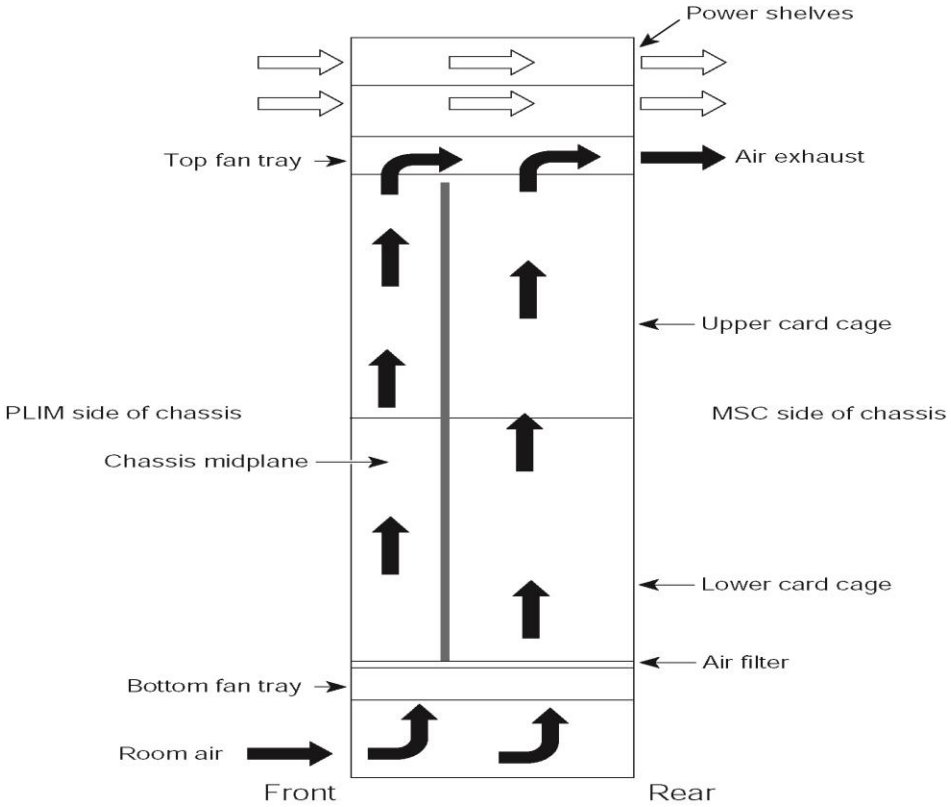
- Power system architecture provides fully redundant AC or DC power
- Line card chassis still operates normally if:
  - One AC rectifier or DC PEM fails
  - One entire power shelf fails, or one bus bar fails
- For system degradation to occur requires two failures:
  - In both the A and B sides of power architecture that effect the same load zone
- Same architecture used for both AC and DC powered line card chassis
- Three different types of power shelves; DC, AC Wye and AC Delta

Status Monitoring

Alarm module responsible for monitoring AC rectifiers or DC PEMs plugged into the power shelf it shares

- The monitored parameters include:
  - Circuit Breaker Tripped conditions
  - Power Good
  - Power Fail
  - Internal Fault
  - Over Temp conditions
  - AC rectifier or PEM presence
  - Voltage and current output levels
- Has a backup power connection to the neighboring power shelf

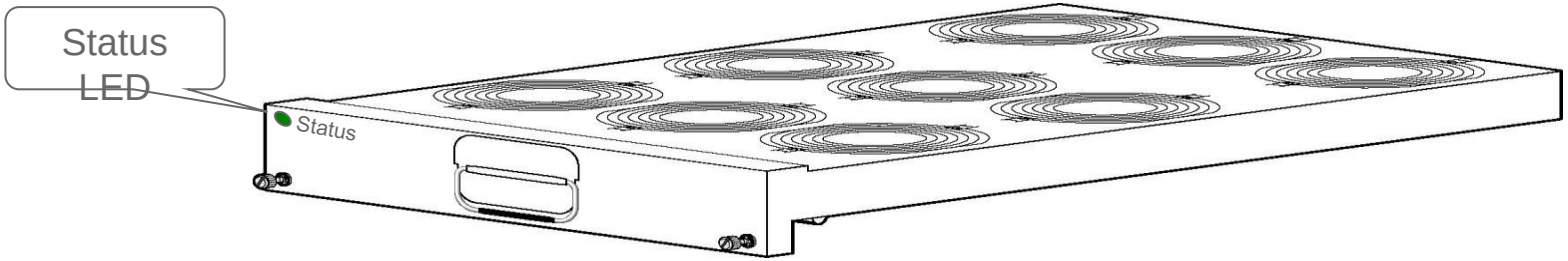
Line Card Chassis Airflow



Fan Control Architecture

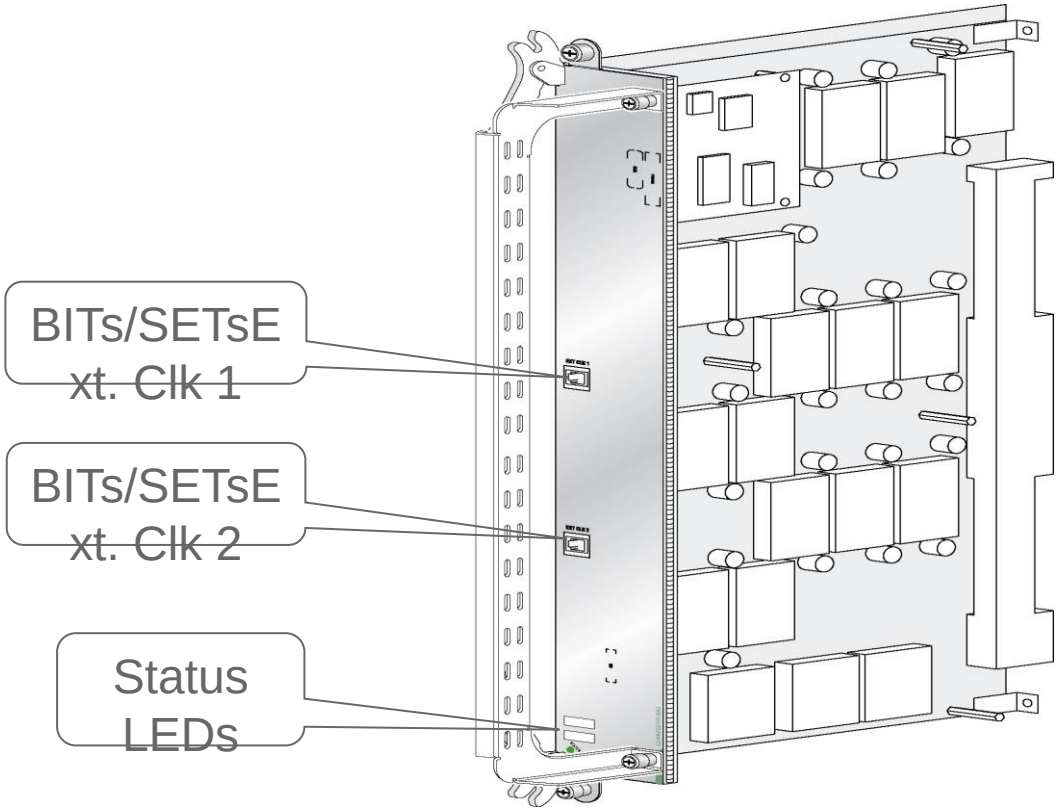
- The fan control architecture:
  - Controls fan speed to optimize cooling, acoustics, and power consumption for various chassis-heating conditions
  - Monitors the cooling system with temperature sensors on modules and cards
  - Is redundant from both a power and cooling standpoint
  - Supports a redundant load-sharing design that contains:
    - Two fan trays, each containing nine fans
    - Two fan controller cards
    - Control software and logic
- There are four normal operating fan-speeds, plus one high-speed setting used when a fan tray has failed.

Line Card Chassis Fan Tray



- The two fan trays:
  - Are interchangeable
  - Plug into the rear of LC chassis
  - Each line card chassis fan tray contains:
    - Nine fans
    - A front-panel status LED

Line Card Chassis Fan Controller Card



Fan Controller Card Operation

- Fans run at 4300 to 4500 RPM at initial power up
- Fan control software takes control of fan speed once the system is initialized (could take 3 to 5 minutes)
- Fan controller cards and fan trays have quick-shutdown mode to aide in OIR
- Quick-shutdown mode minimizes inrush current during hot swap or OIR

Cooling System Redundancy

- The redundancy design in the cooling subsystem can tolerate:
  - A single fan tray failure
  - A single fan failure
  - A single fan controller board failure
  - A single fan cable failure
  - A single power shelf, or a single power module (PEM or AC rectifier) to fail without impacting routing system or line card chassis availability

Thermal Sensors

Thermal sensors on each board in system monitor temperatures throughout chassis

- Three types of sensors in the chassis:
  - Inlet
  - Exhaust
  - Hot spot
- Any sensor can send a thermal alarm
- When thermal alarm occurs fault condition passed to SP on each fan controller board for control software to takes appropriate action

Air Filter Replacement

- The chassis has a replaceable air filter mounted in a slide-out tray above the lower fan tray. The Cisco CRS 16-slot line card chassis air filter plugs into the rear (MSC) side of the chassis.
- You should change the air filter as often as necessary. Before removing the air filter for replacing, you should have a spare filter on hand. Then, when you remove the dirty filter, install the spare filter in the chassis.
- The CRS-16 replacement filters
  - CRS-16-LCC-FILTER => CRS-16S
  - CRS-FCC-FILTER => Fabric Card Chassis
- A lattice of wire exists on both sides of the air filter with an arrow that denotes airflow direction and a pair of sheet metal straps on the downstream side of the filter assembly.

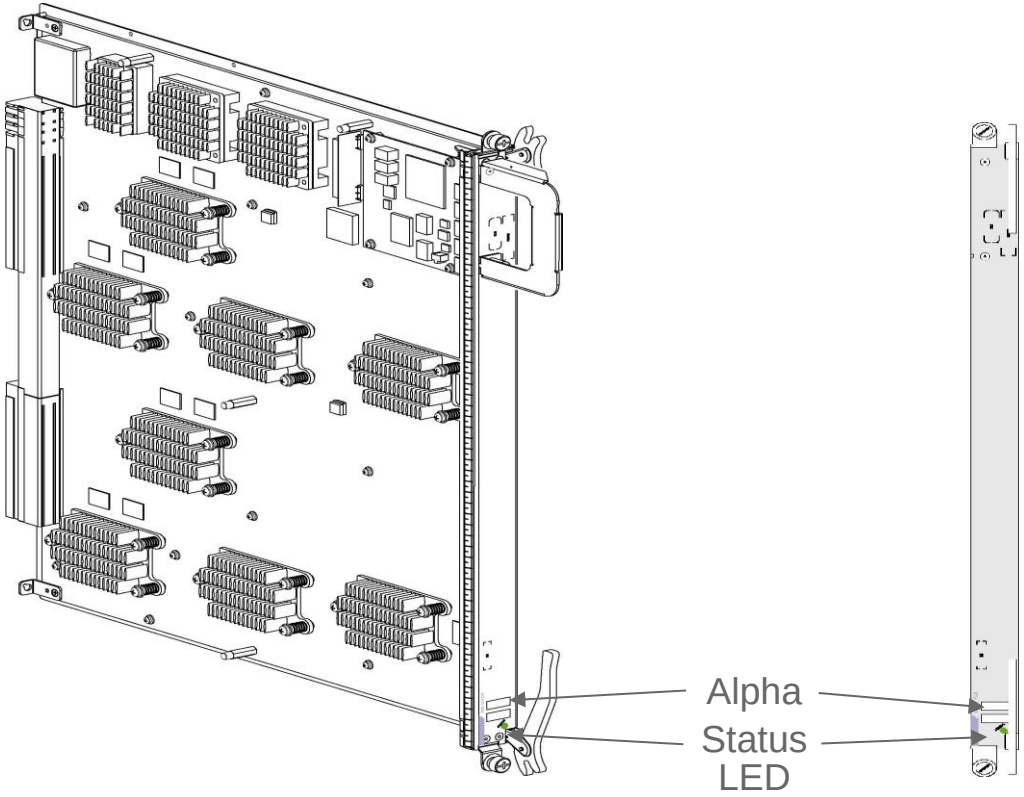
Switch Fabric Overview

- The Cisco CRS routing system fabric is implemented through multiple redundant switch fabric cards (SFCs) installed in the chassis. The switch fabric uses a cell-switched, buffered, three-stage Benes switch fabric architecture. The switch fabric receives user data from a modular services card (MSC) or Forwarding Processing card (FP) and performs the switching necessary to route the data to the appropriate egress MSC or FP.
- A fabric plane on a CRS-3 is made of 3 Switching ASIC Elements (SEA) known as S1, S2, and S3. The only difference between an S1, S2, or S3 is how the ASIC is configured.
- In a standalone chassis, all the elements are contained on a single fabric card .

Switch Fabric Overview (Continued)

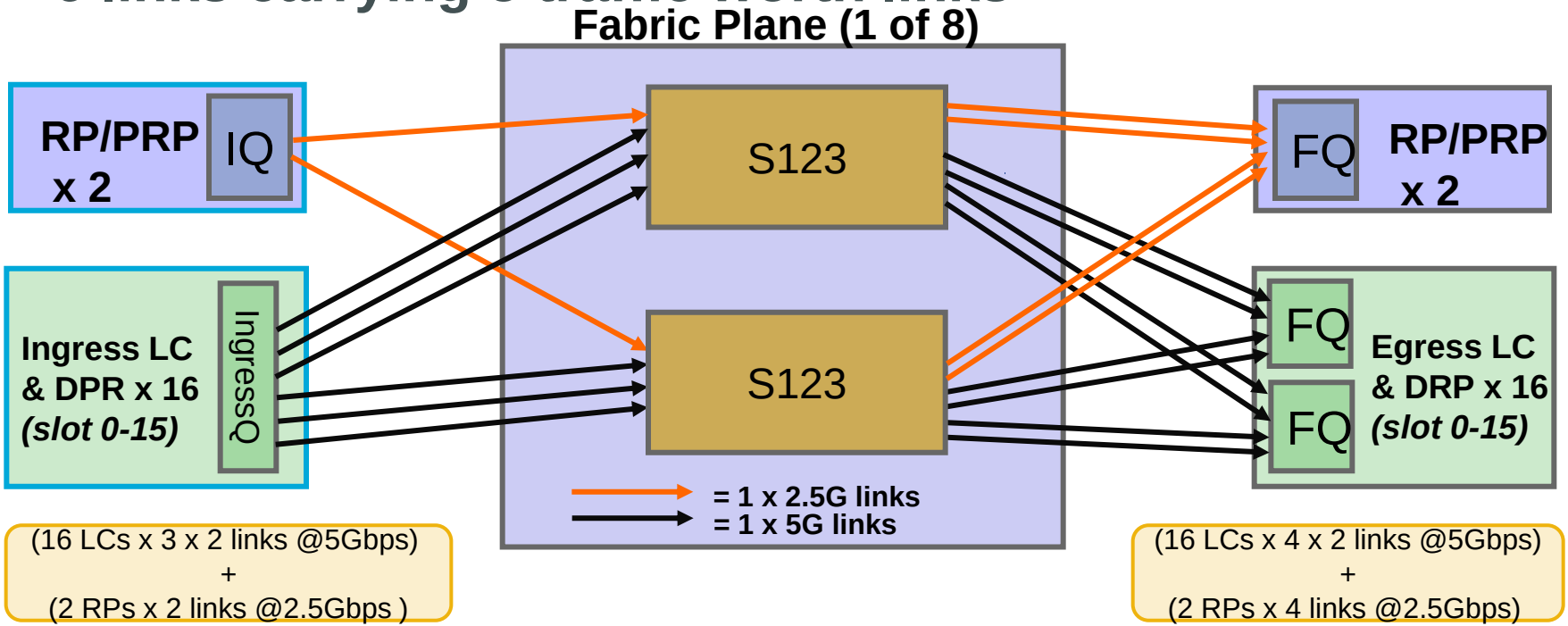
- If the line card chassis (LCC) is operating as a single-shelf (standalone) system, there are two types of switch fabric cards used in the LCC:
  - CRS-16-FC/S (40G)
  - CRS-16-FC140/S (140G)
- The CRS-16-FC140/S fabric is able to operate in both 40G mode and 140G mode to allow interconnection between 20G, 40G, or 140G MSCs and FPs.
- The CRS-1 uses CRS-16-FC/S fabric modules.
- The CRS-3 uses CRS-16-FC140/S fabric modules.

S123 CRS-16-FC/S Physical Overview



CRS-3 16 slots Fabric

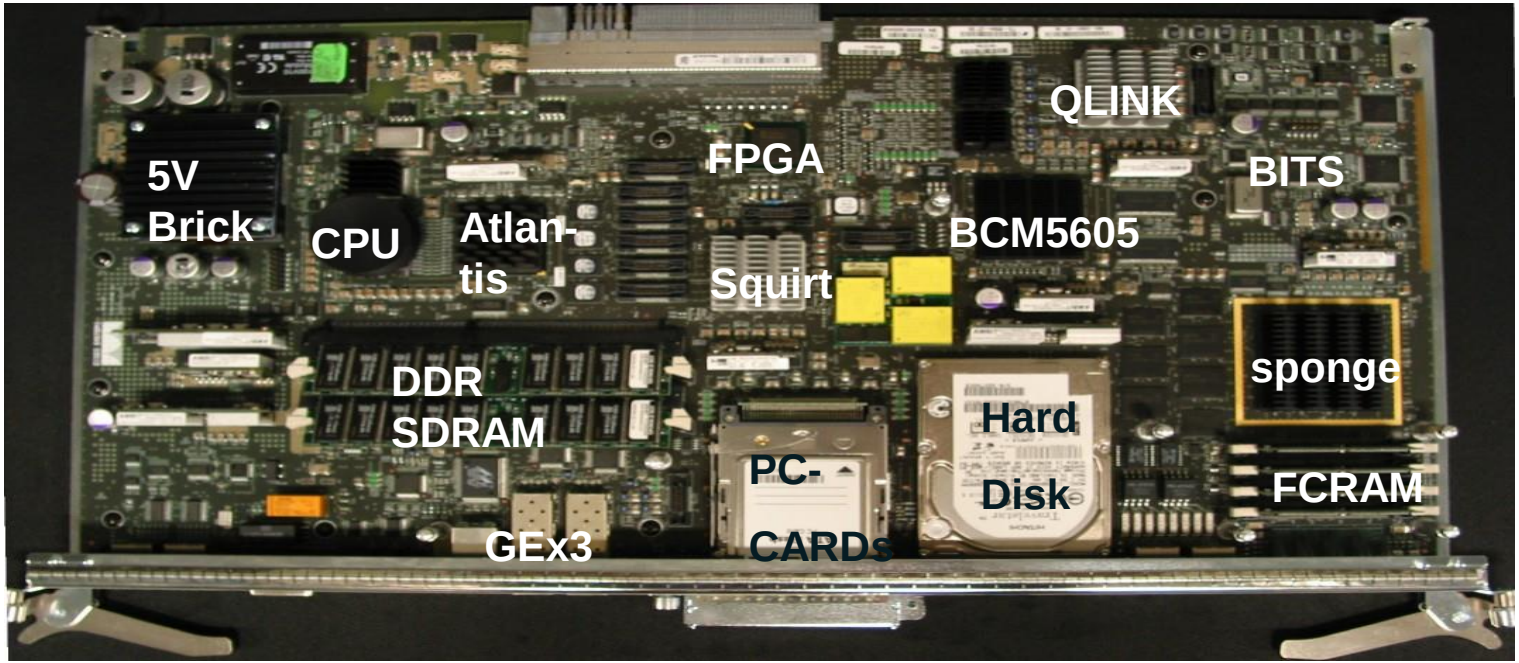
6 links carrying 5 traffic worth links



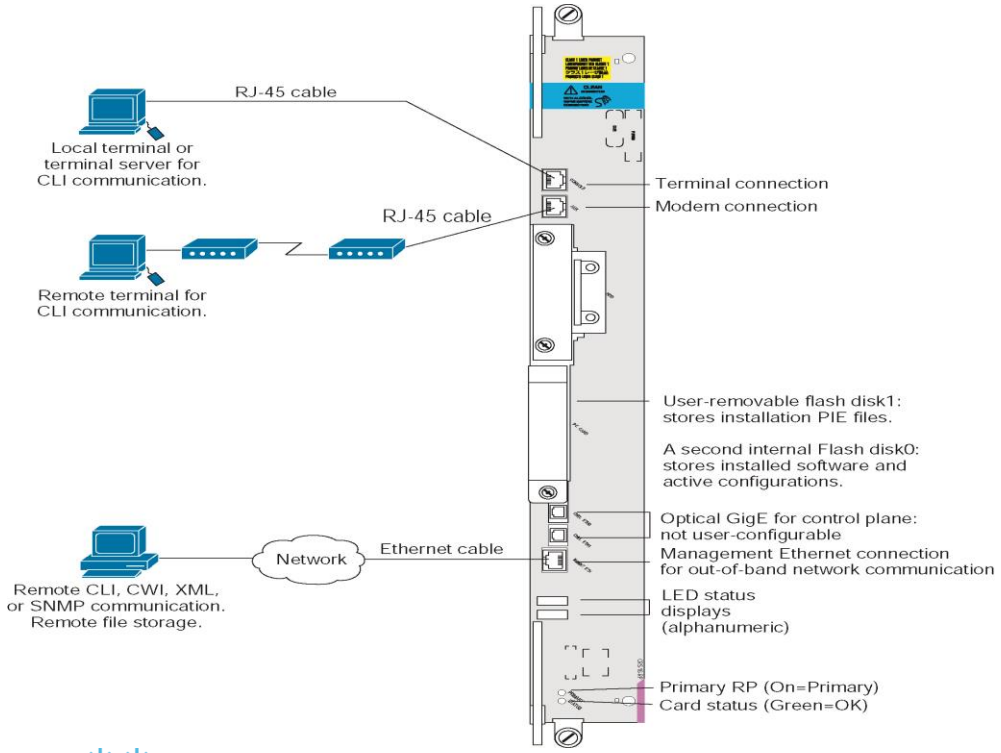
Route Processor (RP) – Overview

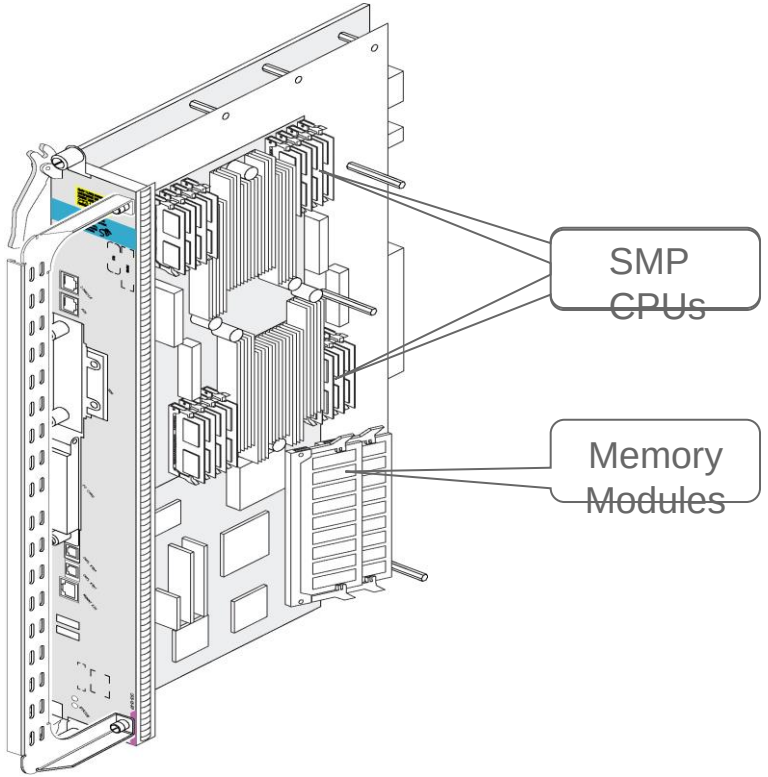
- The RP combines system controller functionality with route processing capability
- Each 16-Slot Line Card Chassis contains two route processor (RP) cards that:
  - One RP serves as the active master, while the other serves as the standby unit
  - Are located in dedicated slots the front side of the chassis in the center of the lower PLIM card cage
  - Distribute forwarding tables to the line cards
  - Provide a control path to each MSC via 100 Mbps FE connection
  - Provide the system-monitoring functions
  - Contain the hard disks for system and error logging

Legacy RP architecture



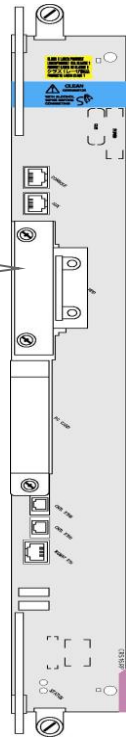
RP Front Panel and Memory Options





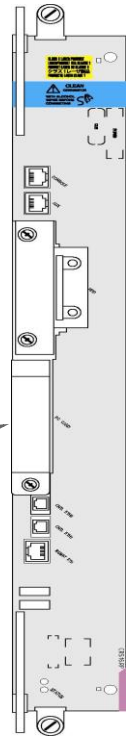
RP Front Panel and Memory Options

- RP IDE hard drive:
  - Used for storing debug info, such as, core dumps from RP or MSCs
  - Typically only active when needed
  - Hot-pluggable and sled mounted



PCMCIA Flash Slots

- PCMCIA Flash
  - Each RP provides two ATA type PCMCIA flash slots to store up to 1 GB storage systems
  - Disk0: is fixed and used for permanent storage of configuration and image files required for operation of OS
  - Disk1: is an externally accessible media slot



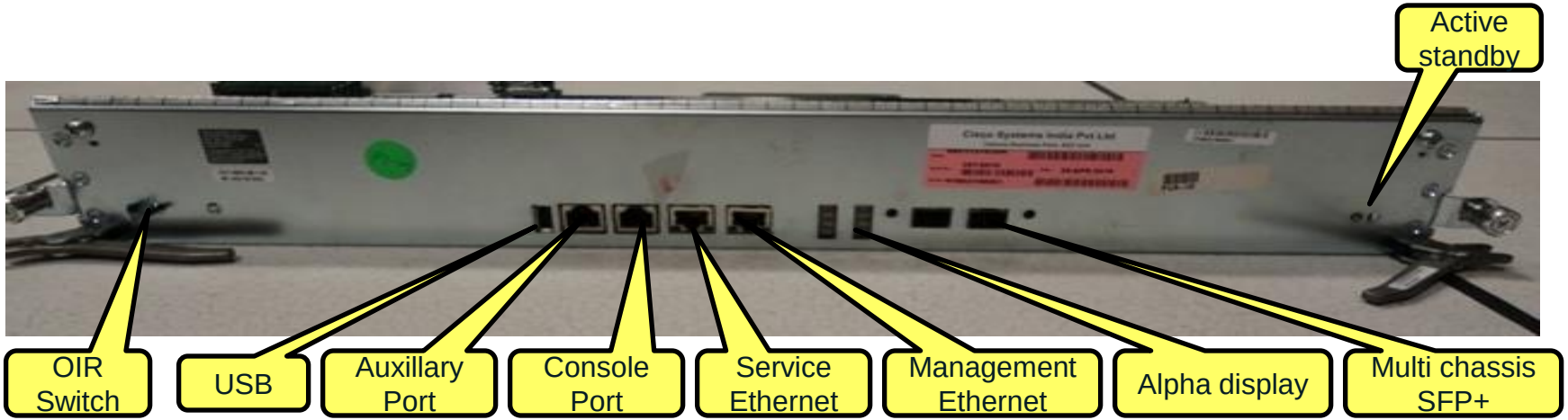
Performance Route Processor (CRS-16-PRP-6G/CRS-16-PRP-12G)

- Performance Route Processor (PRP)
- Intel based Multi-core CPU
- More horse power than PowerPC
- Increased RAM and L1/L2 Cache
- Control Plane / Multi-Chassis Scale
- Faster convergence
- Increase control plane scale
- Improve system performance, serviceability and debugging
- Control plane protection

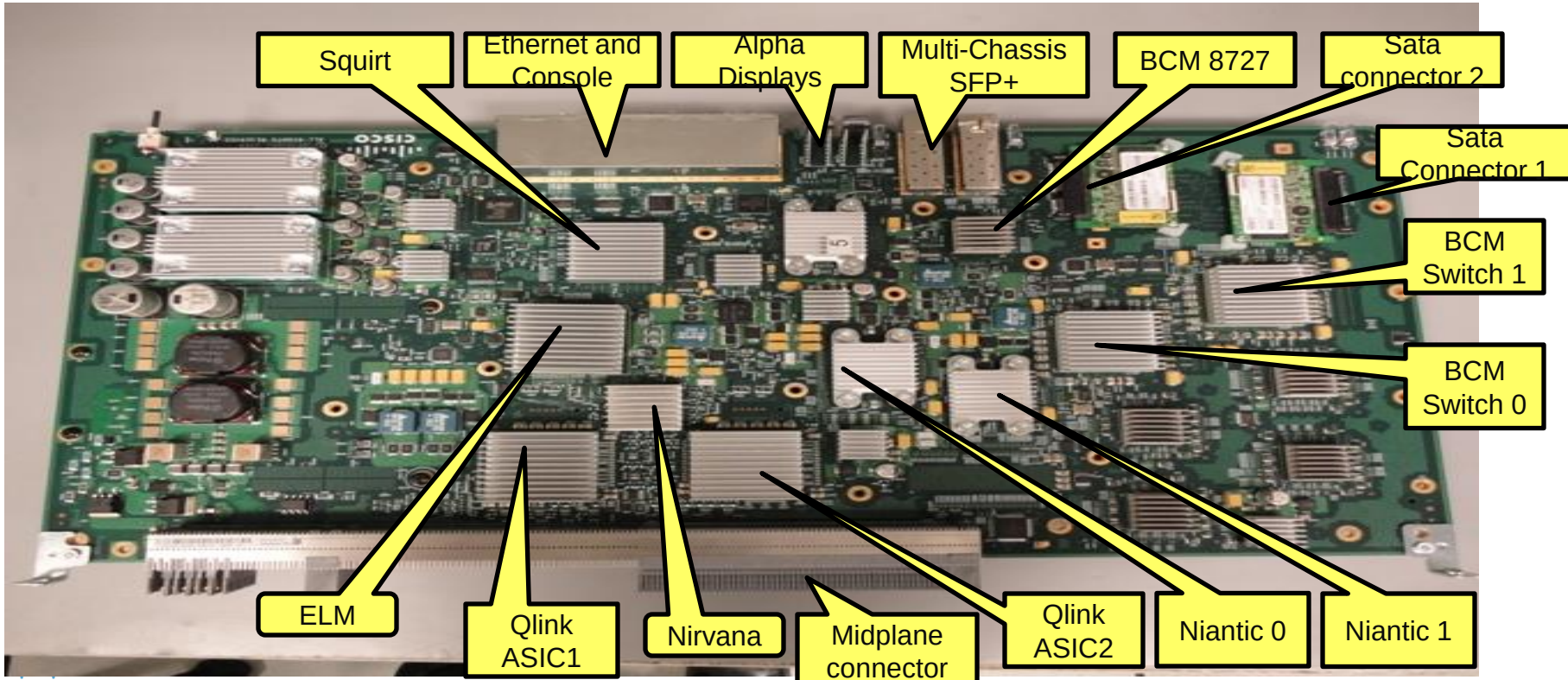
PRP Improved performances

- Larger scales (MC)
- Boot up time improved
- RP failover time improved
- CPU intensive tasks improved (SNMP, …)
- Control plane convergence time improved (Route Reflector)

PRP-16 Front Panel



CRS-16-PRP Mainboard PCB Overview



CRS
4-Slot Line Card Chassis
8-Slot Line Card Chassis

CRS 8 Slot CRS-8-LCC

Midplane design:

- Front
  - 8 PLIM slots
  - 2 RP slots
- Back
  - 8 MSC Slots
  - 4 Fabric cards

Dimensions:

- 17.5” W x 36.6” D x 38.5” H
- (44.5 W x 93 D x 97.8 H cm)

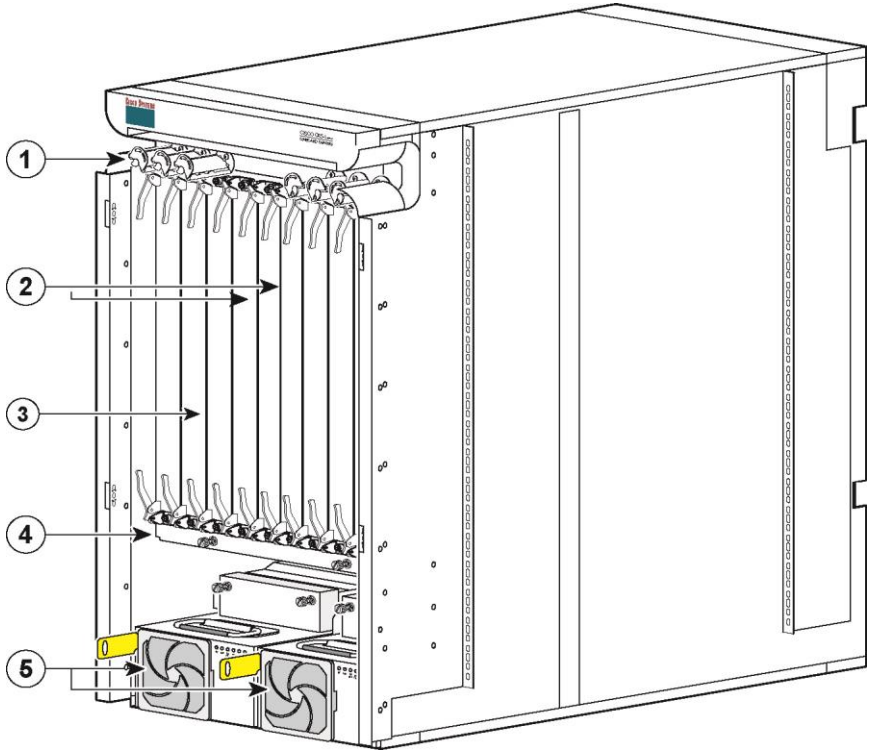
Power: 7.5 KW DC,
8.75 KW AC

Weight: ~ 600 lbs/275kg

Heat Dis.: 27,350 BTU

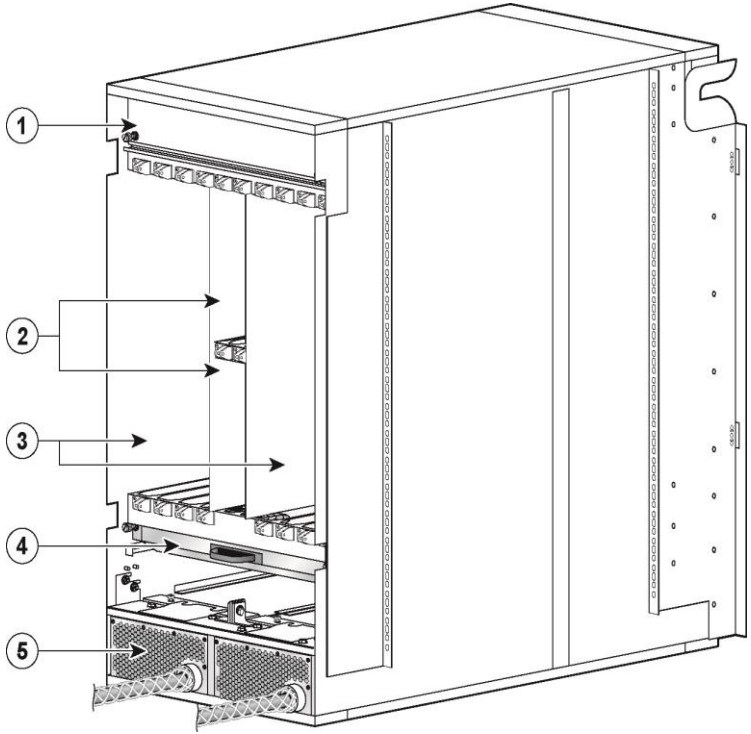
Rack mountable

CRS 8-Slot Line Card Chassis Components – PLIM Side



1. Cable management system
2. Two route processor (RP) cards.
3. PLIMs
4. Air Filter
5. Two AC rectifier modules or two DC power entry modules (PEMs), one for each power distribution unit (PDU).

MSC Side



1. Upper fan tray.
2. Four half-height switch fabric cards (S123).
3. Up to eight modular services cards (MSCs)
4. Lower fan tray.
5. The power system consists of two AC or DC power distribution units (PDUs), and two AC rectifier modules or two DC power entry modules (PEMs), one for each PDU.

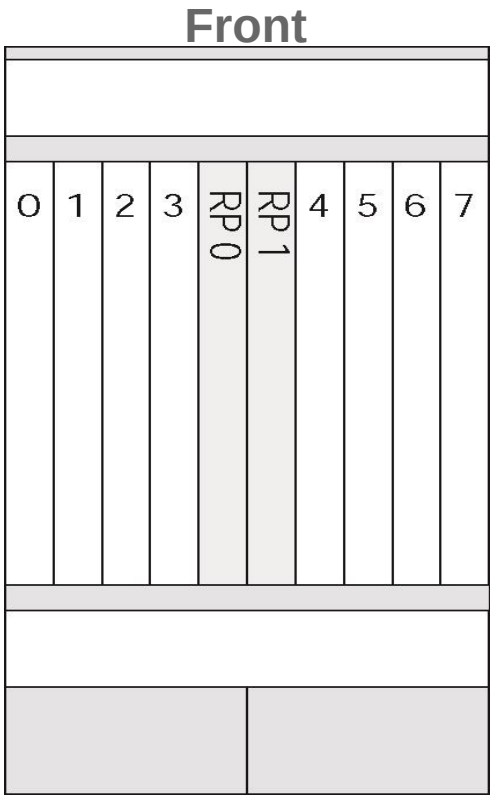
CRS 8-Slot Enhanced Chassis (CRS-8-LCC-B)

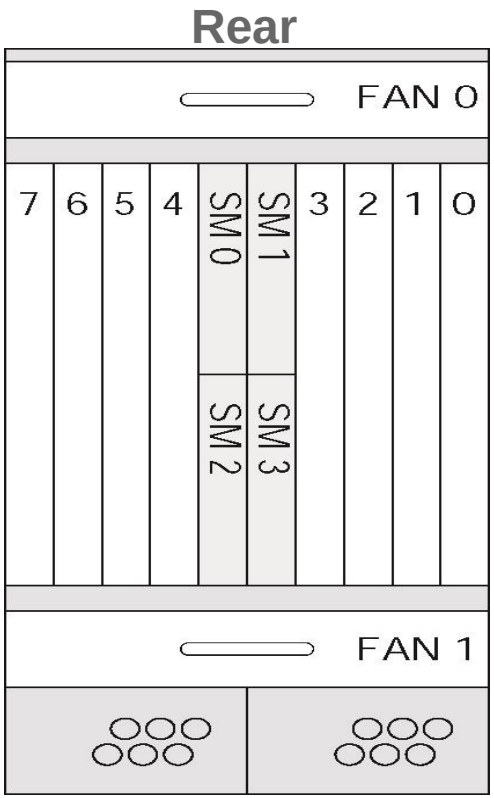
- Cisco IOS XR Software Release 4.1.2 introduces support for the Cisco CRS Series Enhanced 8-slot Line Card Chassis (LCC).
- Each slot has the capacity of up to 400 gigabits per second (Gbps) ingress and 400 Gbps egress, for a total routing capacity per chassis of 12.8 terabits.
- The LCC supports both 40 G and 140 G fabric cards and line cards.
- The Cisco CRS-1 Carrier Routing System uses fabric cards designed for 40 G operation (CRS-8-FC/S or CRS-8-FC/M cards) and the Cisco CRS-3 Carrier Routing System uses fabric cards designed for 140 G operation (CRS-8-FC140/S or CRS-8-FC140/M cards).
- A mixture of 40 G and 140 G fabric cards is not supported except during migration.

CRS 8-Slot Enhanced Chassis (CRS-8-LCC-B) Components

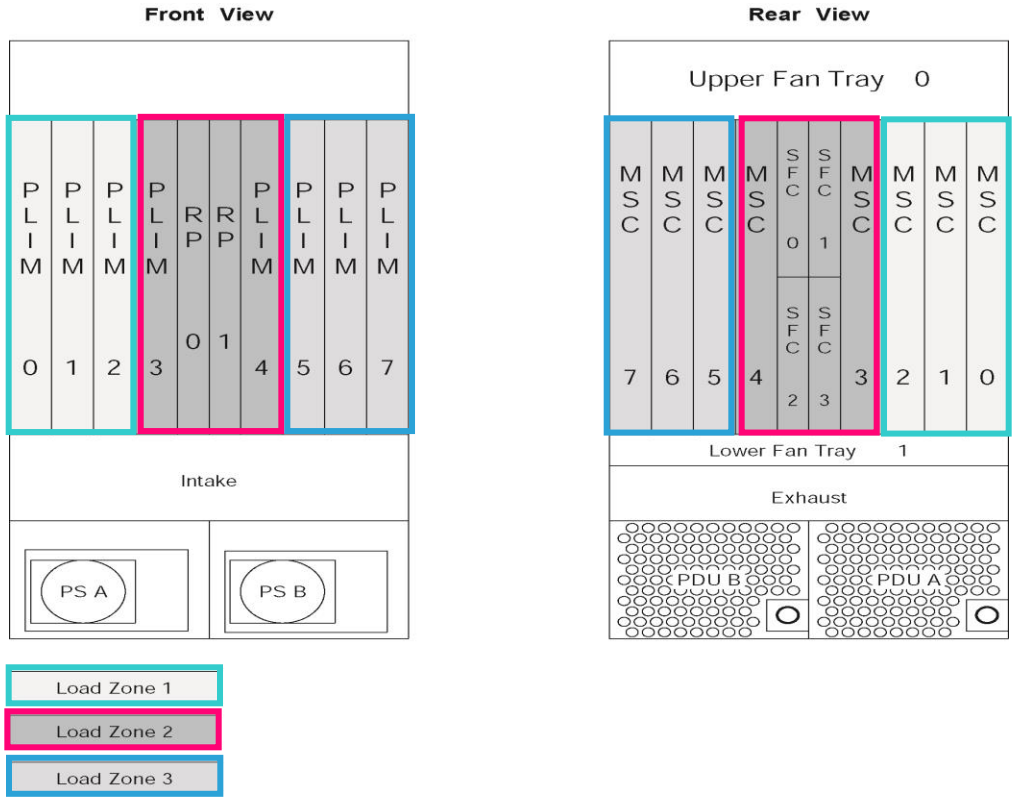
- The CRS-8-LCC-B is supported in Release 4.1.2 to increase the middle plane to 400G per slot and to make necessary changes in thermal and power capacity to support this 400G capacity. This is compatible to support all 40G and 140G cards.
- A new power shelf with an upgraded 70 Amp circuit breaker is created for the 400G chassis to support an increased load of 400G per slot. The changes made in the hardware have created a new Product ID (PID) for the Chassis (CRS-8-LCC-B), and new Modular AC and DC power shelves for the CRS-8-LCC-B.
- CRS Modular DC Power Shelf for CRS-8/S-B (CRS-8-PSH-DC-B)
- CRS Modular AC Power Shelf for CRS-8/S-B (CRS-8-PSH-AC-B)
- The CRS-8-LCC-B supports only modular power modules.

CRS 8-Slot Line Card Chassis Slot Numbering





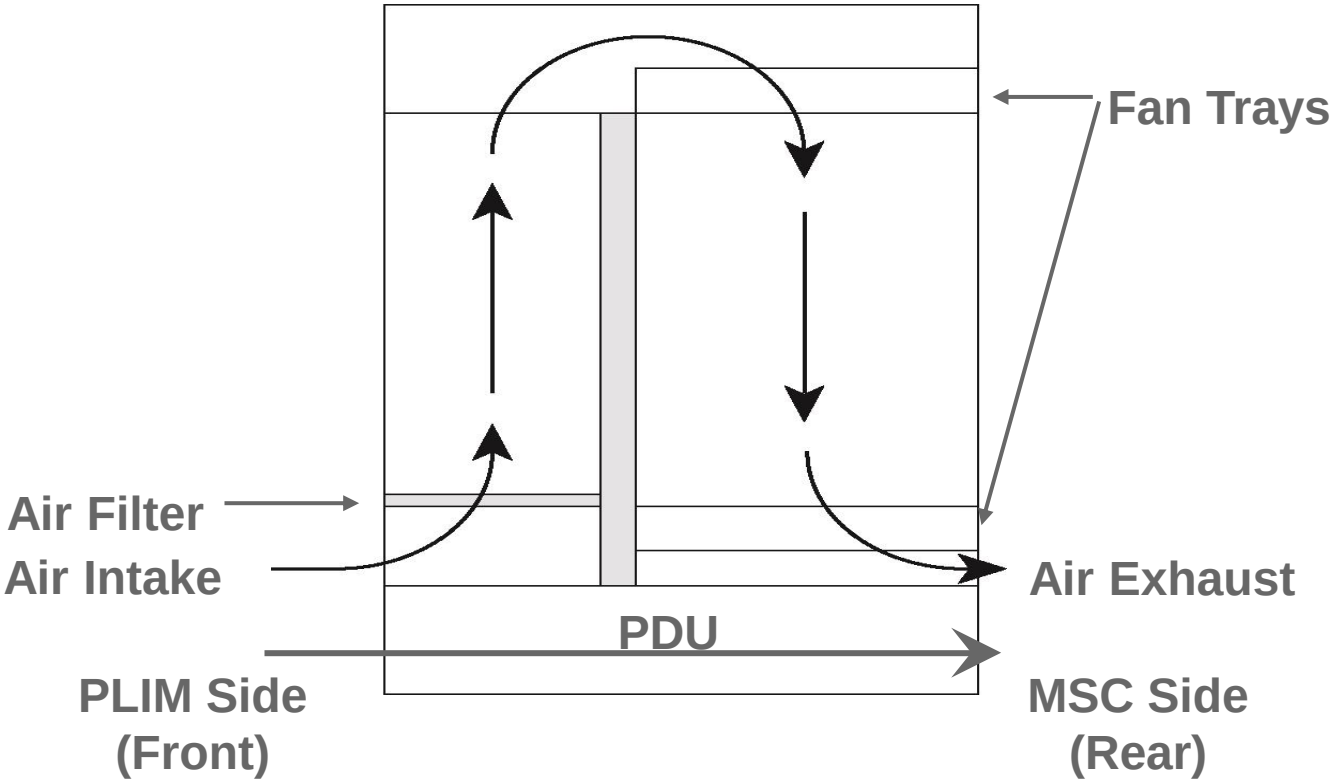
Chassis Load Zones



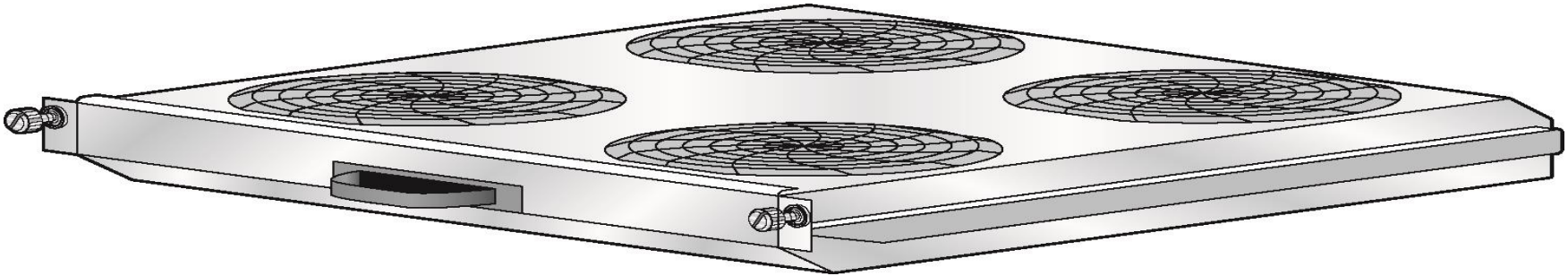
CRS 8-Slot Line Card Chassis Cooling System

- Cooling system fully redundant allows for single-fault failure
- Complete cooling system includes:
  - Two fan trays
  - Temperature sensors
  - Control S/W and logic
  - Air Filter, inlet/outlet air vents & bezels
  - Impedance carriers
- 4 fans in each tray operate as a group
- Thermal sensors located throughout chassis
- S/W runs on SP to control fan operations
- SP modules connected via internal Ethernet to SC on RP

Line Card Chassis Airflow & Air Filter

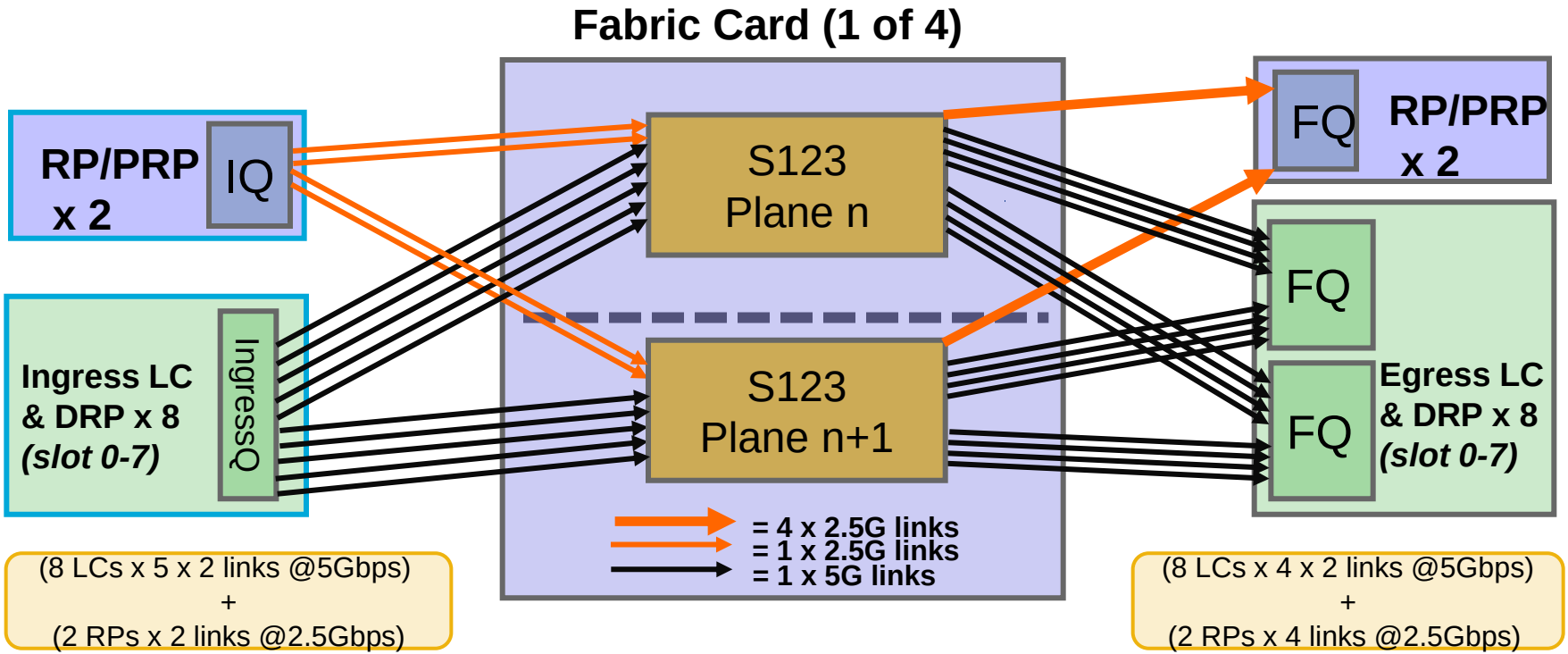


Fan Tray



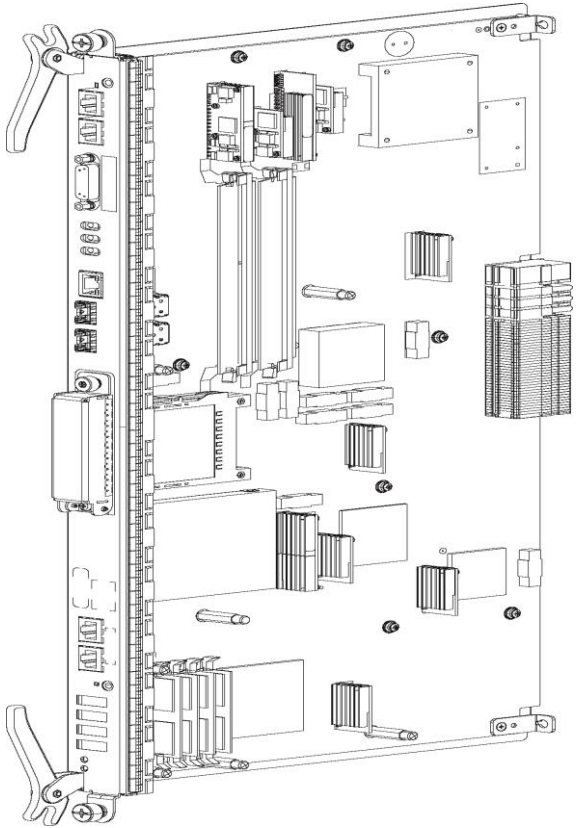
- Each fan tray:
  - Has 4 +24 VDC fans
  - Fan speeds range from 4000 to 6700 RPM
  - Fan tray board
  - Front-panel status LED
-

CRS-3 8 slots Fabric (CRS-8-FC140/S)



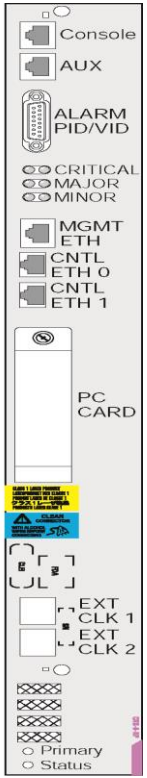
CRS-1 8-slot Line Card Chassis RP Overview

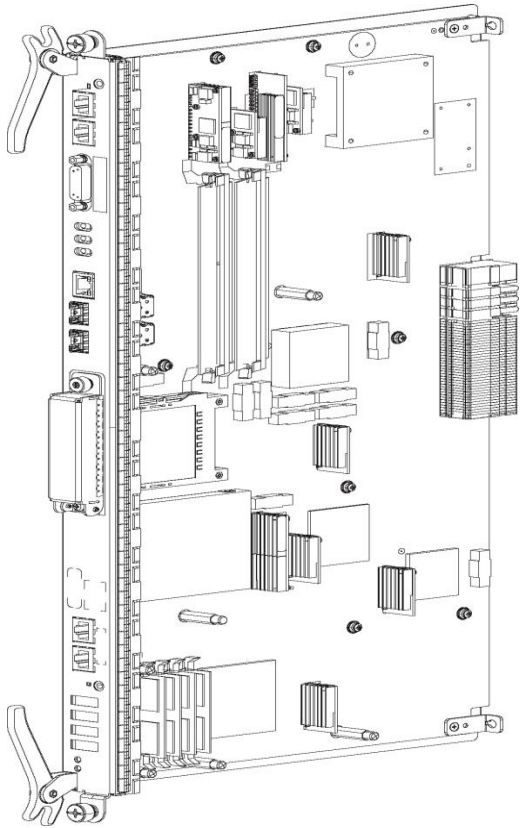
- Not interchangeable with 16 slot RP
- Single MPC7457 (1.2Ghz) processor
- 2 RPs required for redundancy
- Route processing functionality
- System Controller functionality
- Alarm, fan and power supply controller functionality
- Also used in the 4-slot CRS chassis



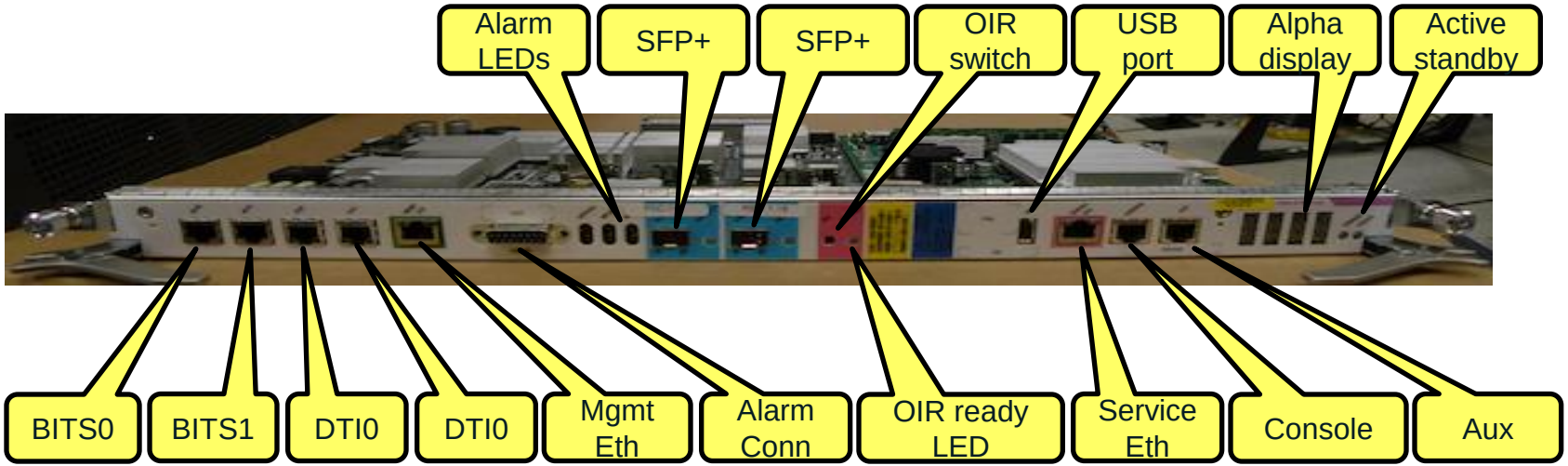
RP Components (CRS-8-RP/CRS-8-RP-B)

- Hard drive – 40 Gig.
- Memory 2 or 4 GB
- 2 PCMCIA slots
- CPU
- 2 SPF Modules
- RJ45 Ethernet port
- Fast Ethernet Midplane Connector

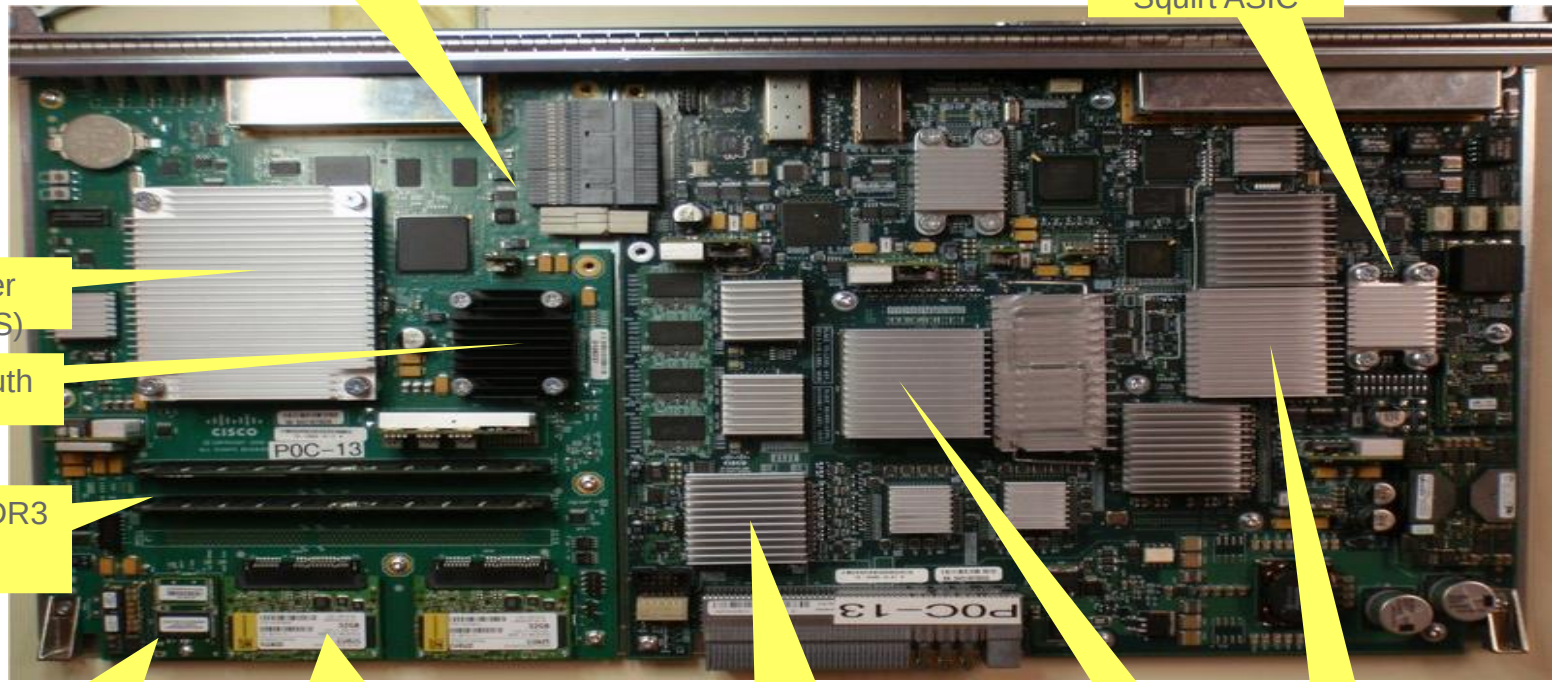




PRP-8 Front Panel



PRP-8 Overview

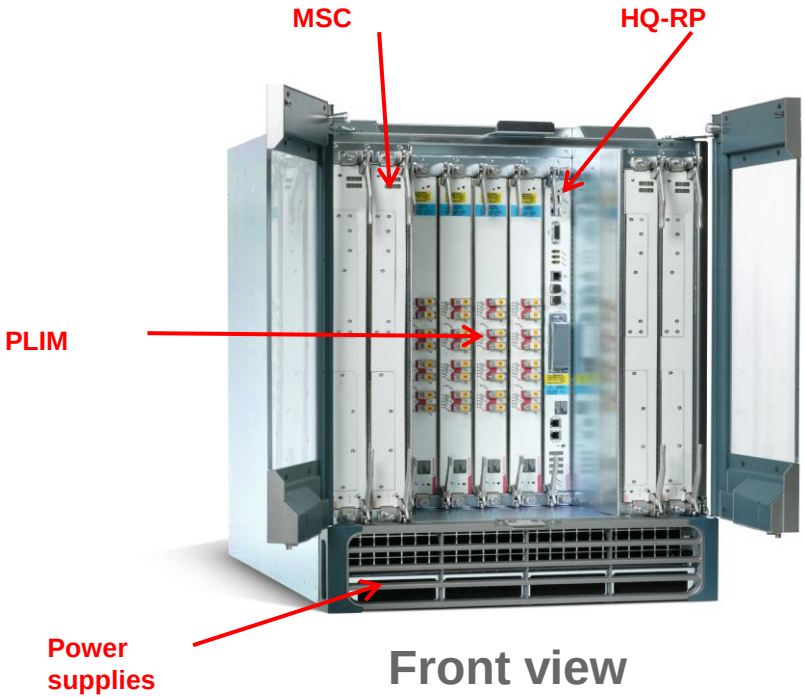


System Overview 4-slot Chassis

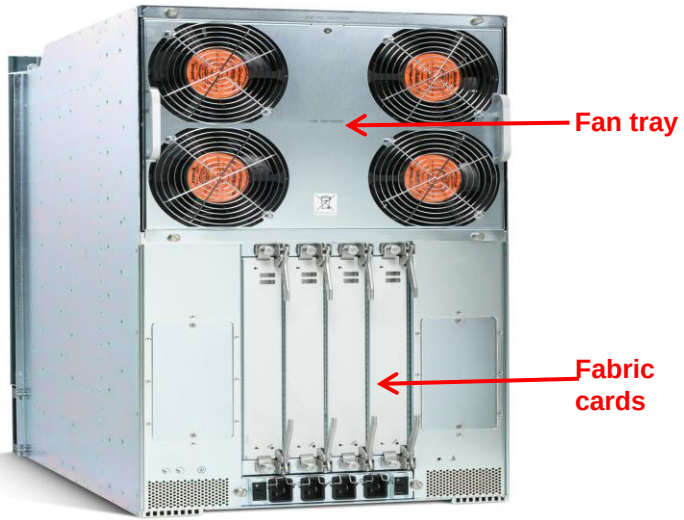
- The 4 slots configuration for the CRS systems family
- 30” x 30.28” x 18.5” (height x depth x width)

- **Hardware configuration:**
  - 4 Line cards and PLIM cards
  - 2 RP cards – Uses same RPs as 8-slot chassis
  - 4 Fabric cards
  - 1 Power shelf (4 power modules)
  - 1 Fan tray

System Overview 4-slot Chassis

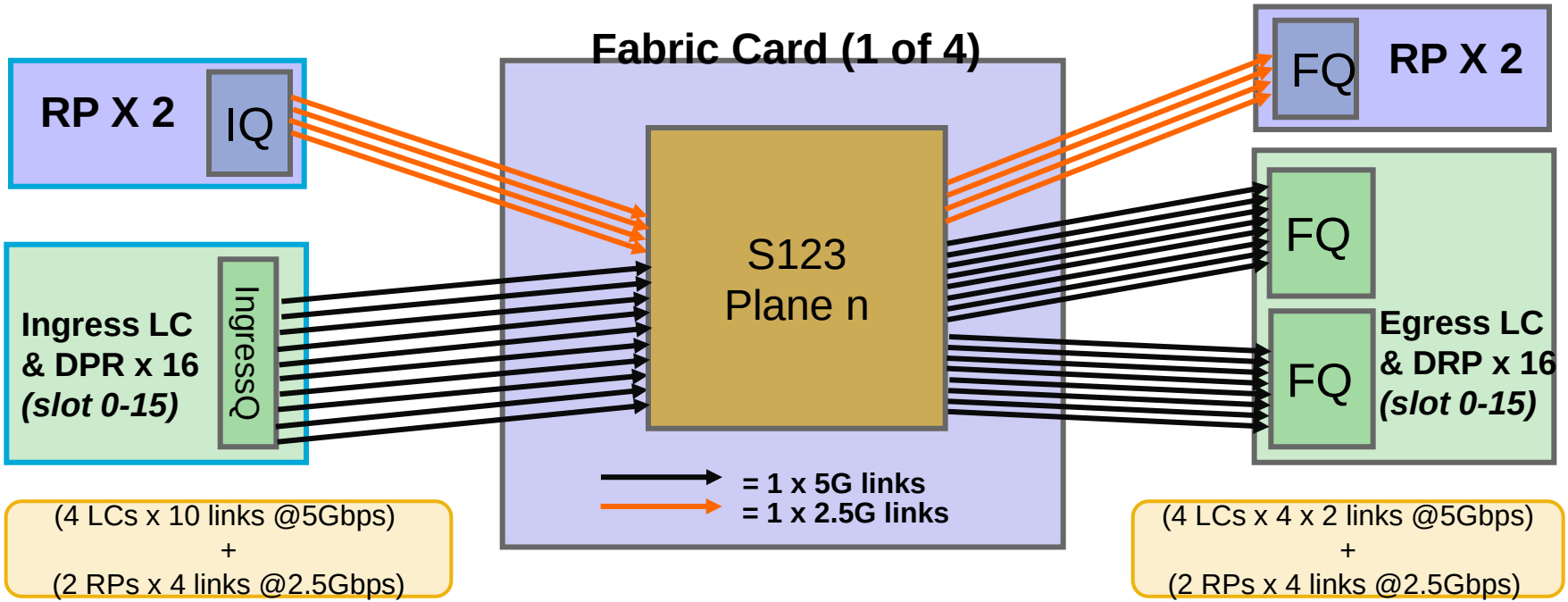


Front view



Rear view

CRS-3 4-slot Fabric (CRS-4-FC140/S)



Fan Tray 4-slot Chassis

```
RP/0/RP1/CPU0:firefly(admin)#show env
fans
Fan speed (rpm):
       FAN1    FAN2    FAN3    FAN4
Rack 0:
Upper  3487    3487    3508    3487
```

- Minimum speed = 3500rpm
- Maximum speed = 7500rpm
- OIR procedure:
  - Remove fan tray
  - Wait 10 sec
  - Re-insert fan tray
  - If fan tray not re-inserted within 45 seconds, system will shut down

Temperature range (deg C)		Fan speed (rpm)
-	28	3500
27	32	4000
31	36	4500
35	40	5100
39	43	5800
42	46	6500
45	-	7500

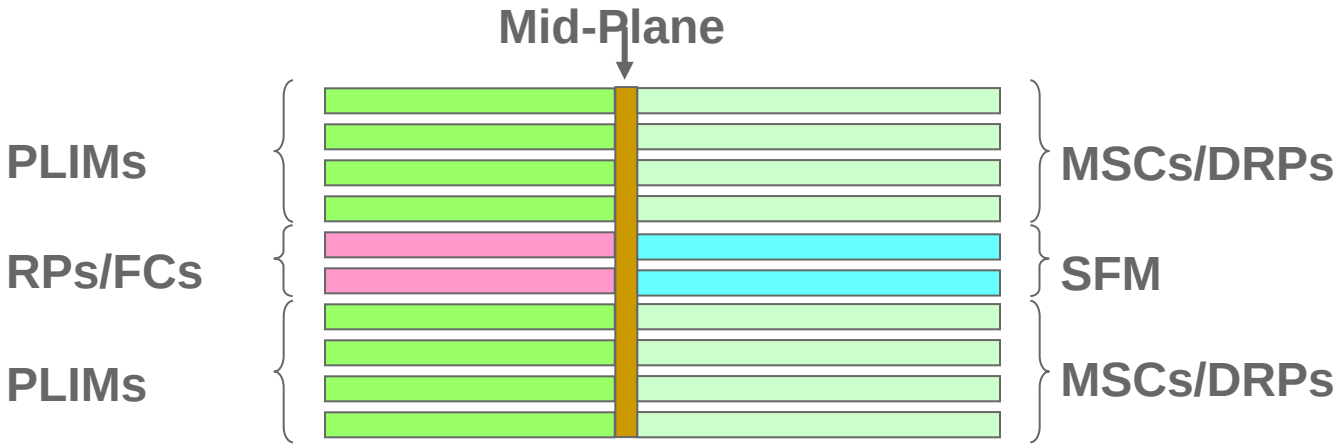
CRS Line Card Chassis Common Elements

Modular Services Cards

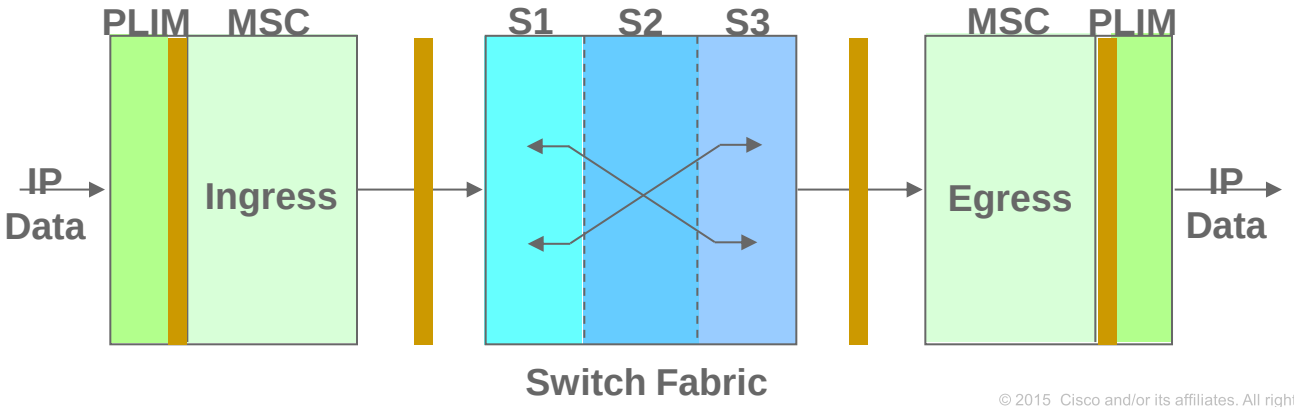
- The Cisco CRS-1 and CRS-3 Modular Services Card is a high-performance Layer 3 forwarding engine. Each MSC is equipped with two high-performance, flexible Cisco SPPs, one for ingress and one for egress packet processing. The card is responsible for all packet processing, including quality of service (QoS), classification, policing, and shaping.
- Each line card is separated by a midplane into two main components: the interface module and the MSC. Each Cisco CRS-1 and CRS-3 line card maintains a distinct copy of the adjacency table and forwarding information databases, enabling maximum scalability and performance.

Packet Flow Summary / Physical & Logical views

Physical View



Logical View



CRS-3 Modular Services Card 140G (CRS-MSC-140G)

- 140 Gbps line rate distributed forwarding
- Compatible with CRS-3 line-card chassis
- Compatible with all current Cisco CRS-1 line-card chassis with 140G fabric cards
- Compatible with 1X100GBE, 14X10GBE-WL-XFP & 20X10GBE-WL-XFP interface modules
- Requires release 4.0.0 PX or later
- High speed edge applications
- Supports up to 64,000 queues and 12,000 interfaces in hardware
- Dual Core MPC8641D CPU with 4GB RAM on a daughter board named “Kensho”.
- 4GB route table memory. Configurable with up to 8 GB of route table memory
- 1 GB of packet buffer memory per side (2 GB total per line card [ingress and egress]

CRS-3 Forwarding Processor (CRS-FP140)

- 140 Gbps line rate distributed forwarding
- Compatible with CRS-3 line-card chassis
- Compatible with all current Cisco CRS-1 line-card chassis with 140G fabric cards
- Compatible with 1X100GBE, 14X10GBE-WL-XFP & 20X10GBE-WL-XFP interface modules
- Requires release 4.0.0 PX or later
- Core Peering Applications
- Supports up to 8 queues per port
- Supports 250 interfaces/subinterfaces
- Configurable with up to 8 GB of route table memory
- 1 GB of packet buffer memory per side (2 GB total per line card [ingress and egress]
- MSC140 and FP140 are physically similar cards from an architectural / ASIC point of view

CRS-3 Label Switch Processor (CRS-LSP)

- 140 Gbps line rate distributed forwarding engine
- Compatible with CRS-3 line-card chassis
- Compatible with all current Cisco CRS-1 line-card chassis with 140G fabric cards
- Compatible with 1X100GBE, 14X10GBE-WL-XFP & 20X10GBE-WL-XFP interface modules
- Optimized for label switching functions in a service provider's network
- Requires release 4.1.1 PX or later
- Support for up to 8 queues per port
- 4GB of route table memory
- Configurable with up to 8 GB of route table memory
- 1 GB of packet buffer memory per side (2 GB total per line card [ingress and egress]
- MSC140 and LSP are physically similar cards from an architectural / ASIC point of view

CRS-3 Line Cards (MSC, FP)

Q&A

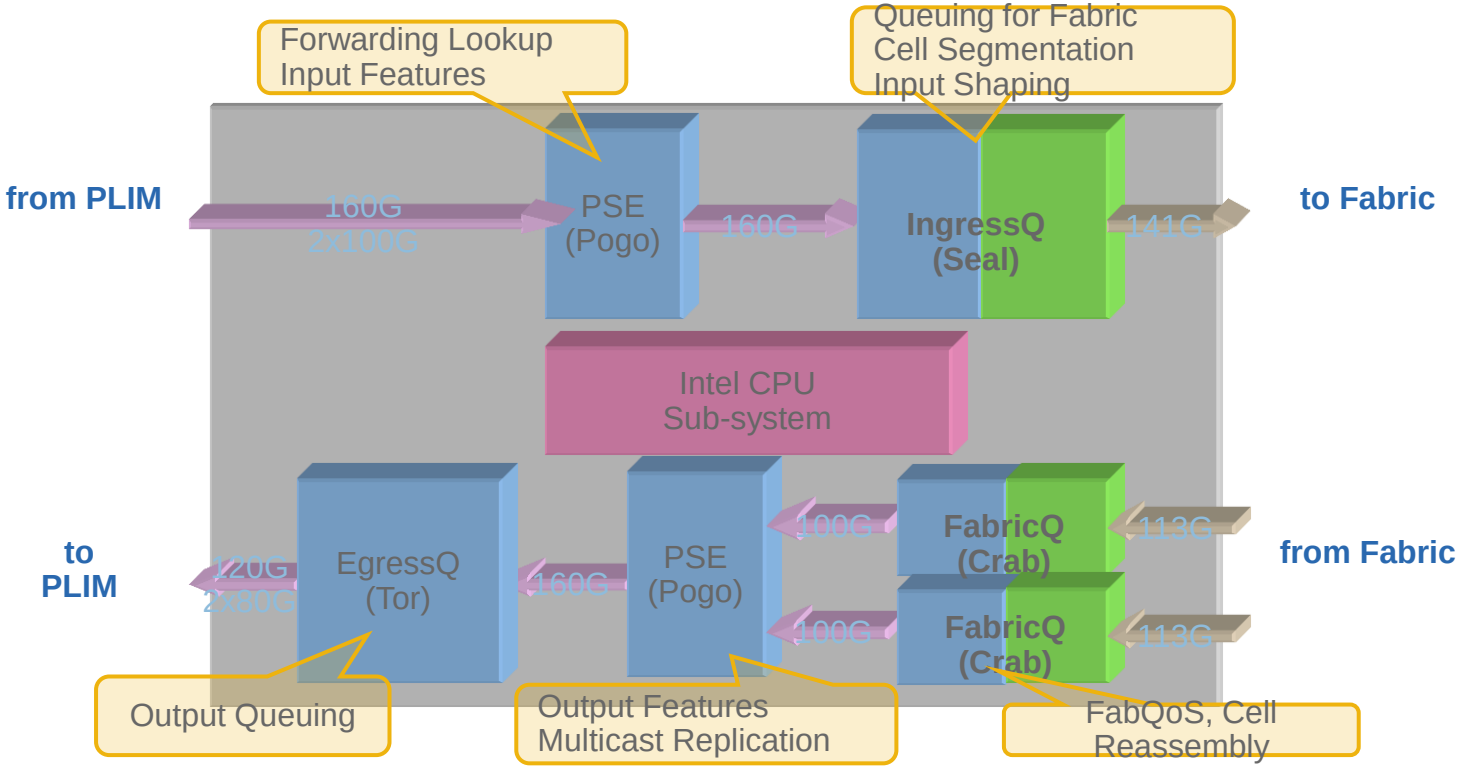
Pergunta 2: Qual é a principal função da ASIC IngressQ de uma MSC?

(a) Encaminhamento e validação de features de input

(b) Enfileiramento e segmentação de células

(c) Validação de features de output e replicação de pacotes multicast

CRS-3 Line Card



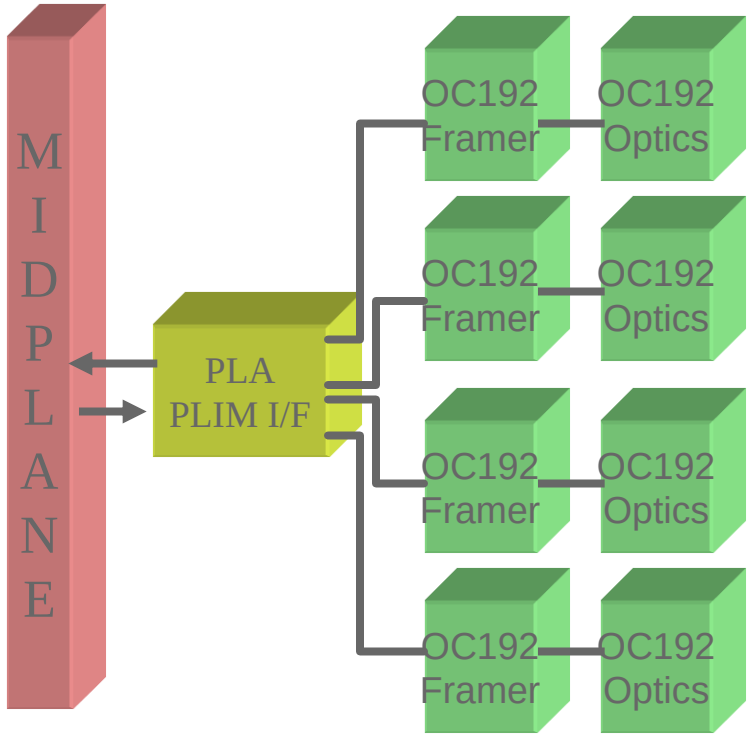
Physical Layer Interface Module

- PLIM provides Layer 1 and Layer 2 services and an interface for routing system
- Optic modules on PLIM contain ports to connect fiber-optic cables
- PLIMs perform:
  - Framing
  - Clock recovery
  - Serialization and de-serialization
  - Channelization
  - Conversion between optical signals and electrical signals
- MSCs and PLIMs installed on opposite sides of line card chassis and mate through chassis midplane
- Chassis midplane enables you to remove and replace an MSC w/o disconnecting user cables on PLIM

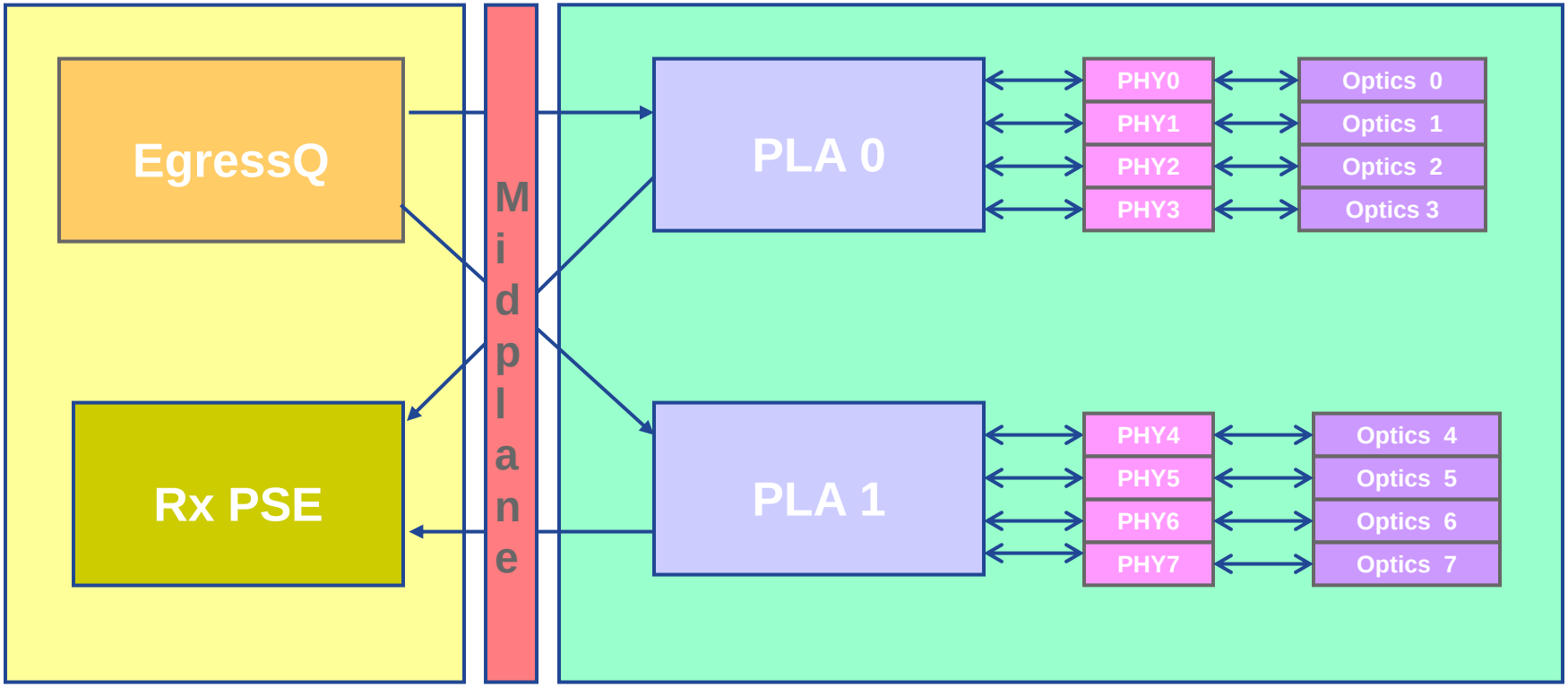
PLIM Functionality

PLA - L2 ASIC

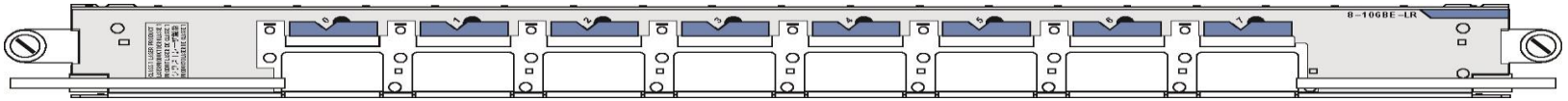
- Some L2 statistics gathering
- Consolidation of port streams for Rx PSE
- Stream separation on Tx
- Ingress monitoring Rx – Buffers for congestion
- Exact PLA variant and number of PLAs varies from PLIM to PLIM



8 – Port 10GE PLIM HW Architecture



8 – Port 10-GE PLIM Faceplate

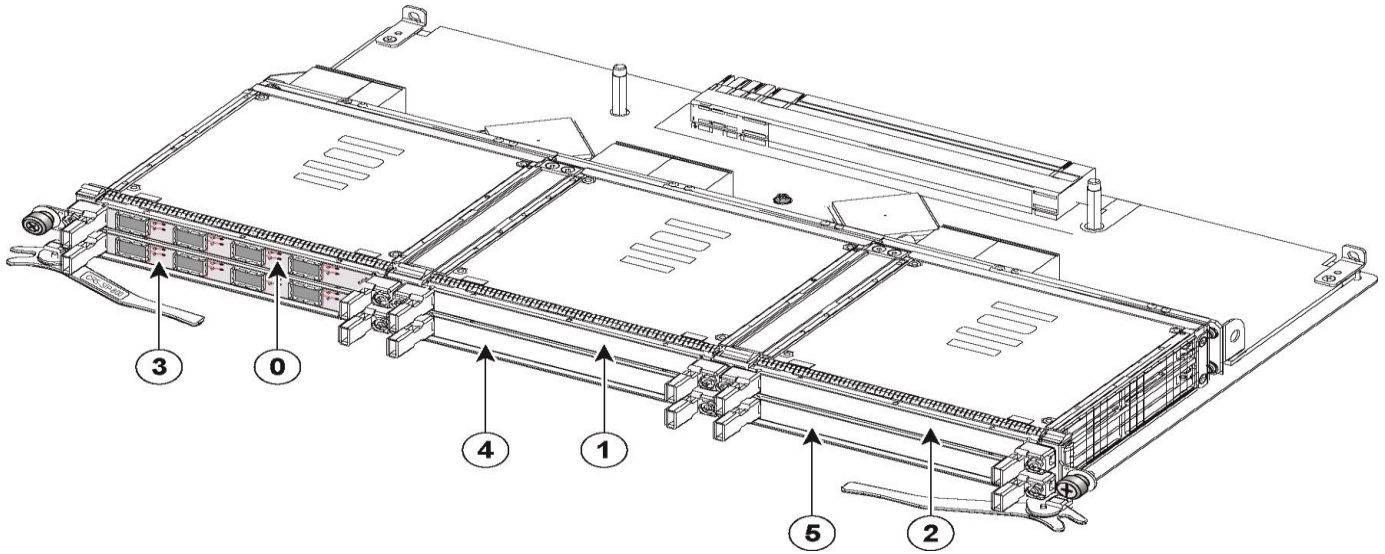


- Eight slots that accept XENPAK optic modules, which provide LR optics with SC fiber-optic interfaces.
- STATUS LED
  - Green indicates that the PLIM is properly seated and operating correctly
  - Yellow or amber indicates a problem with the PLIM
  - Off (dark), check that the board is properly seated and that system power is on
- A LED for each port—Indicates that the port is logically active; the laser is on
- Power consumption—110 W (with 8 optic modules)

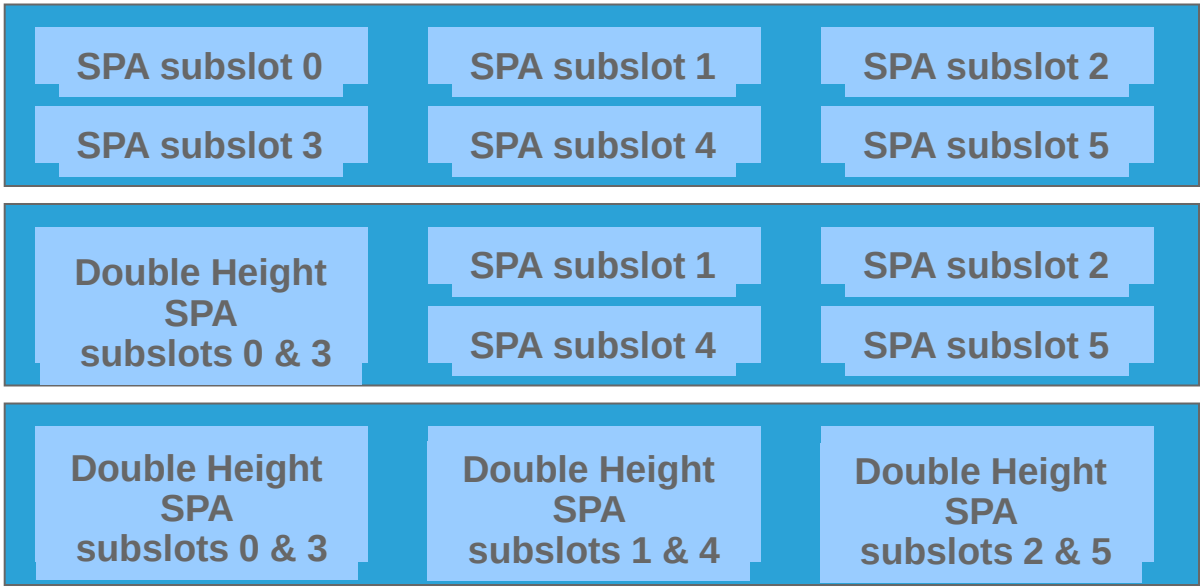
SPA Interface Processor (SIP)

- A SIP is a carrier card similar to PLIM
  - Inserts into line card chassis slot like any other PLIM
  - SIPs provide no network connectivity on their own
- A SIP contains subslots used to house one or more SPAs
  - SPA provides interface ports for network connectivity
- During normal operation SIP should reside in router fully populated with functional SPAs or with a blank filler plate inserted in all empty subslots
- SIPs support online insertion and removal (OIR), while SPAs are inserted in subslots

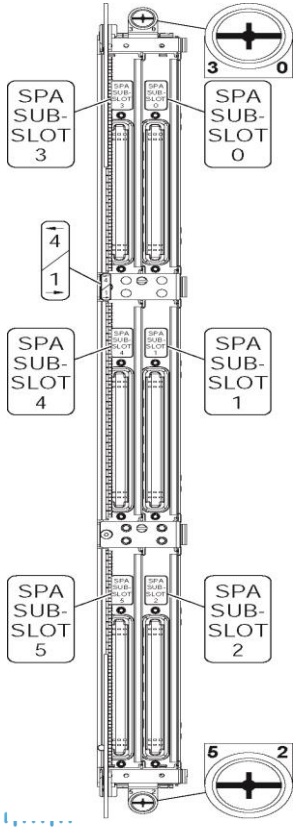
SPA Slot Numbering CRS-1 SIP-800



Shared Port Adapters (SPAs)

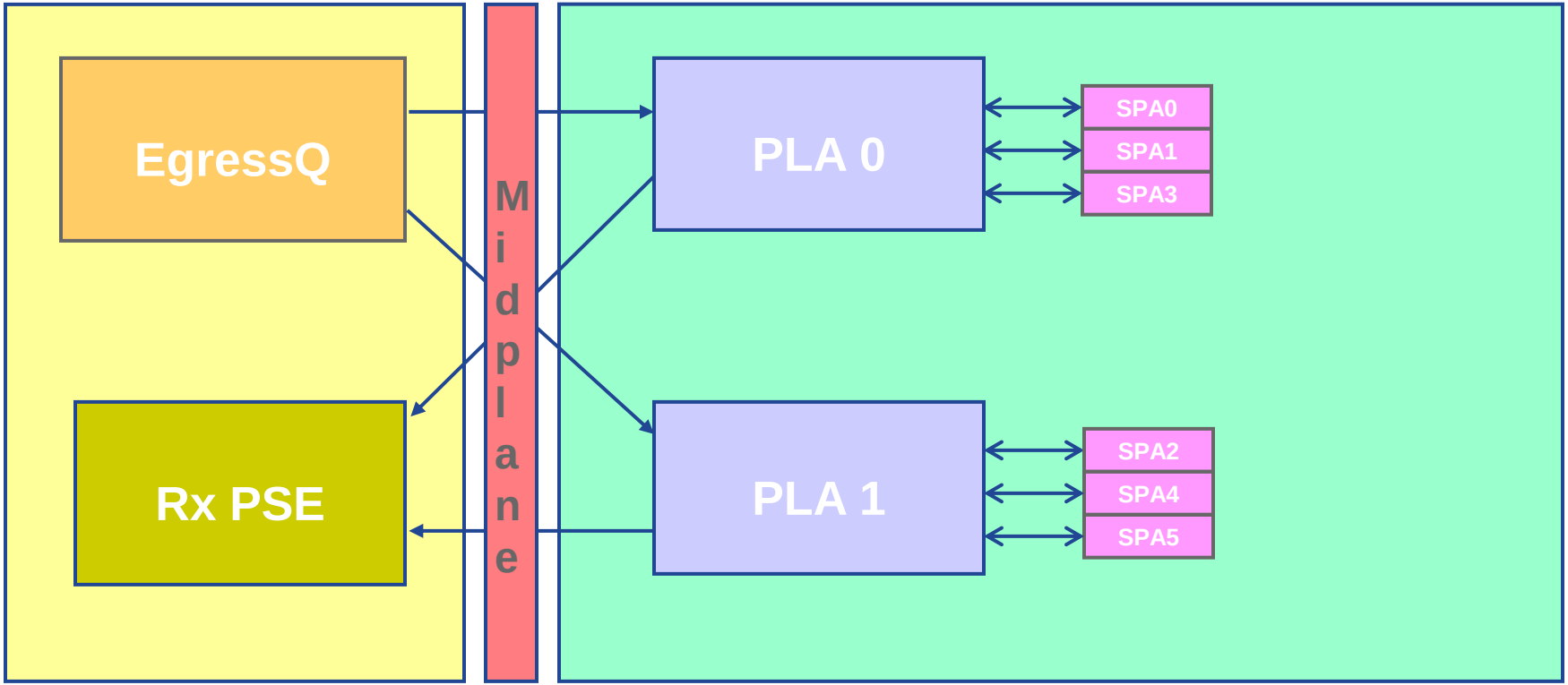


SPA Interface Addresses on SIPs



- A CRS-1 single line card chassis system contains a SIP-800 installed in PLIM slot 4.
- A 4-Port OC-3 POS SPA installed in subslot 3.
  - **Port 2 of that SPA would be addressed as *int pos0/4/3/2*.**

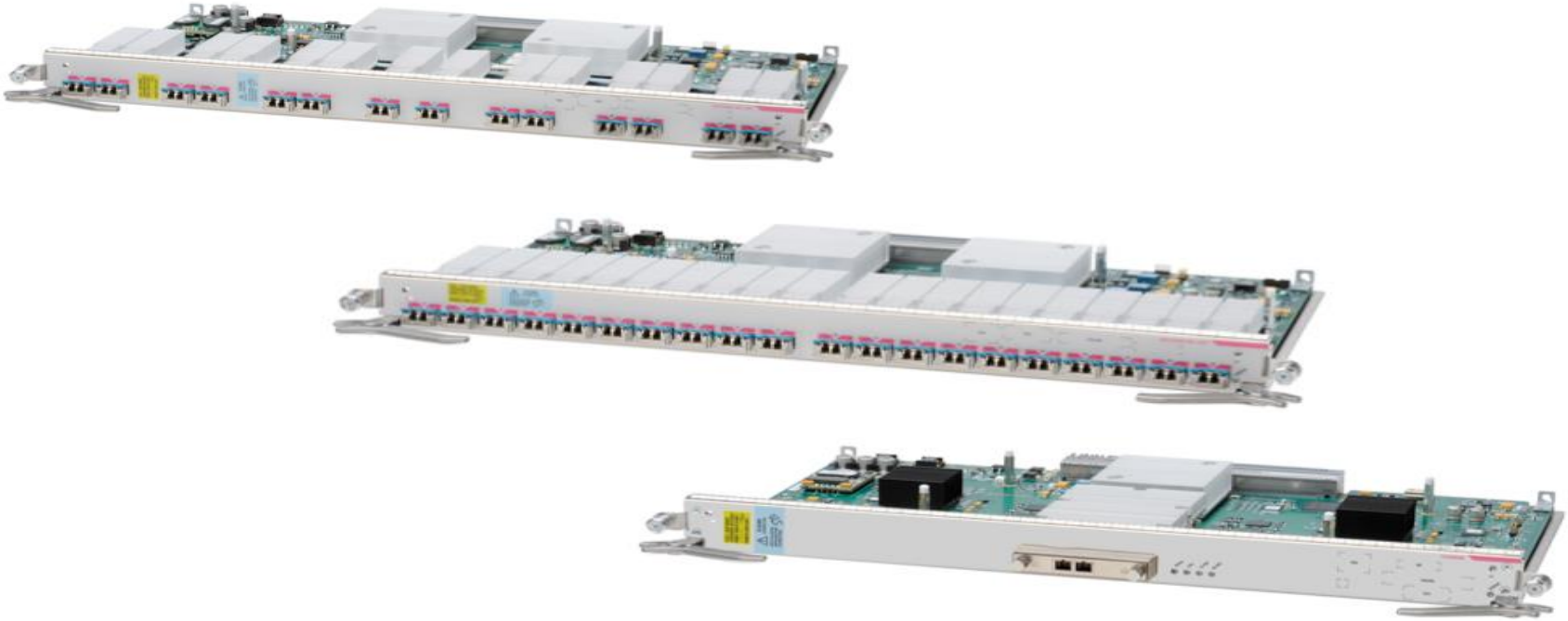
Bandwidth Oversubscription



Bandwidth Oversubscription

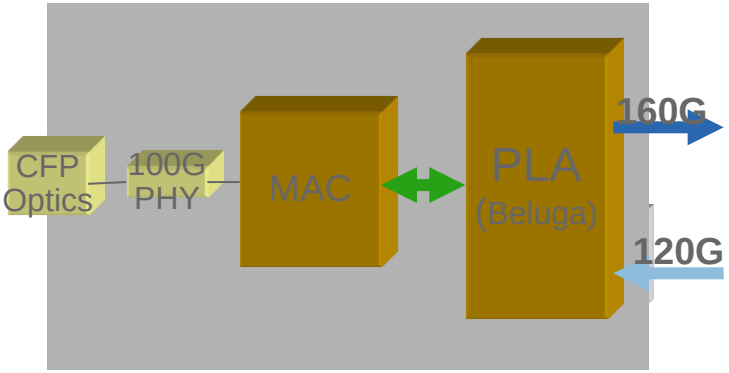
- Allows oversubscription of Gigabit Ethernet Interfaces
- Each PLA handles 20 GB
- Oversubscription is not allowed when any POS SPAs are installed in the SIP. When a SPA is installed that will oversubscribe the PLA the SPA will not power up and you will receive an error message.
- When installing SPAs make sure that the total bandwidth used by all SPAs doesn't exceed 40GB
- When installing SPAs make sure that the total bandwidth of the SPAs in subslots 0, 1, and 3 doesn't exceed 20GB
- When installing SPAs make sure that the total bandwidth of the SPAs in subslots 2, 4, and 5 doesn't exceed 20GB

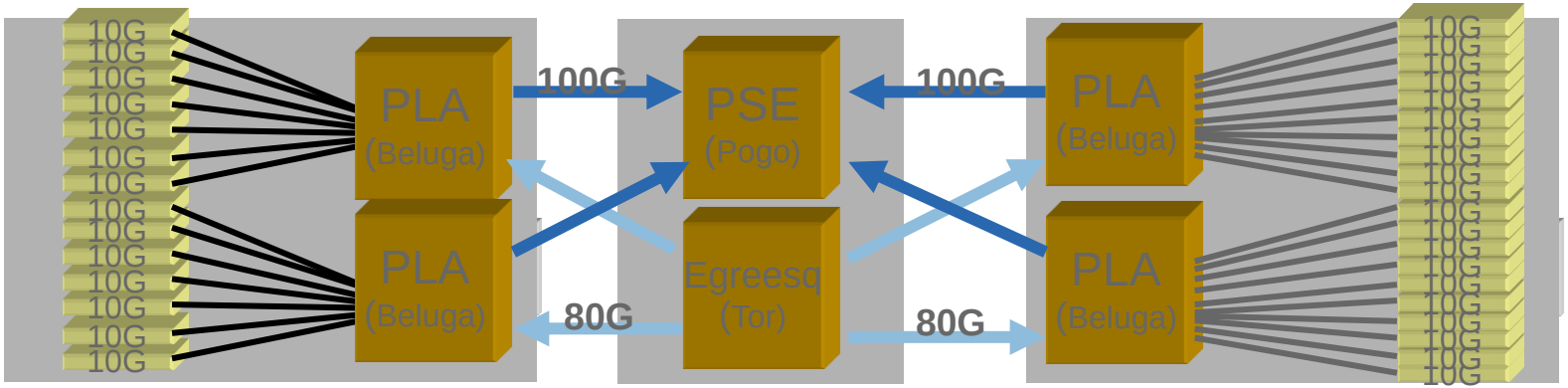
CRS-3 PLIMs



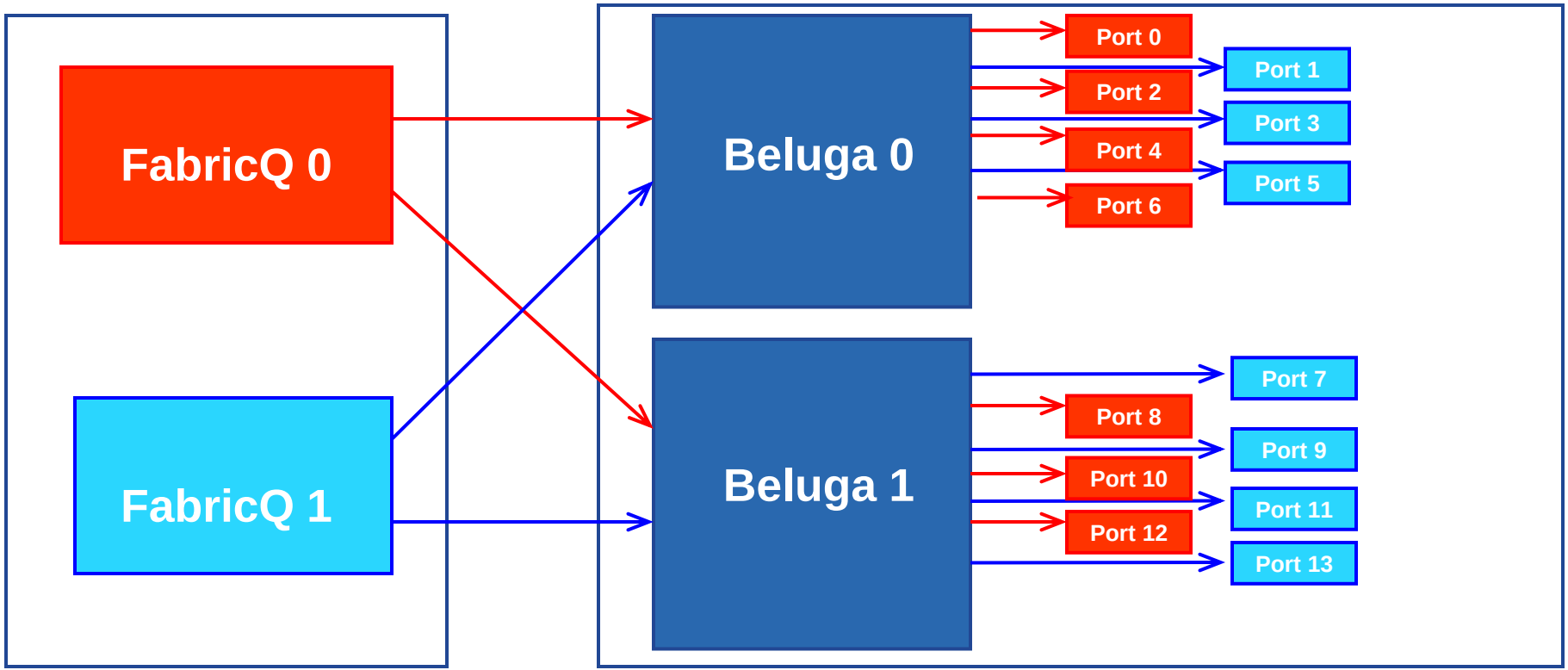
CRS-3 PLIMs

- Three PLIMs offered at FCS
  - 1x100GE, 14x10GE, 20x10GE
- Ethernet OAM support at hardware level
- Supports low-power XFPs
  - Part # includes “-L”

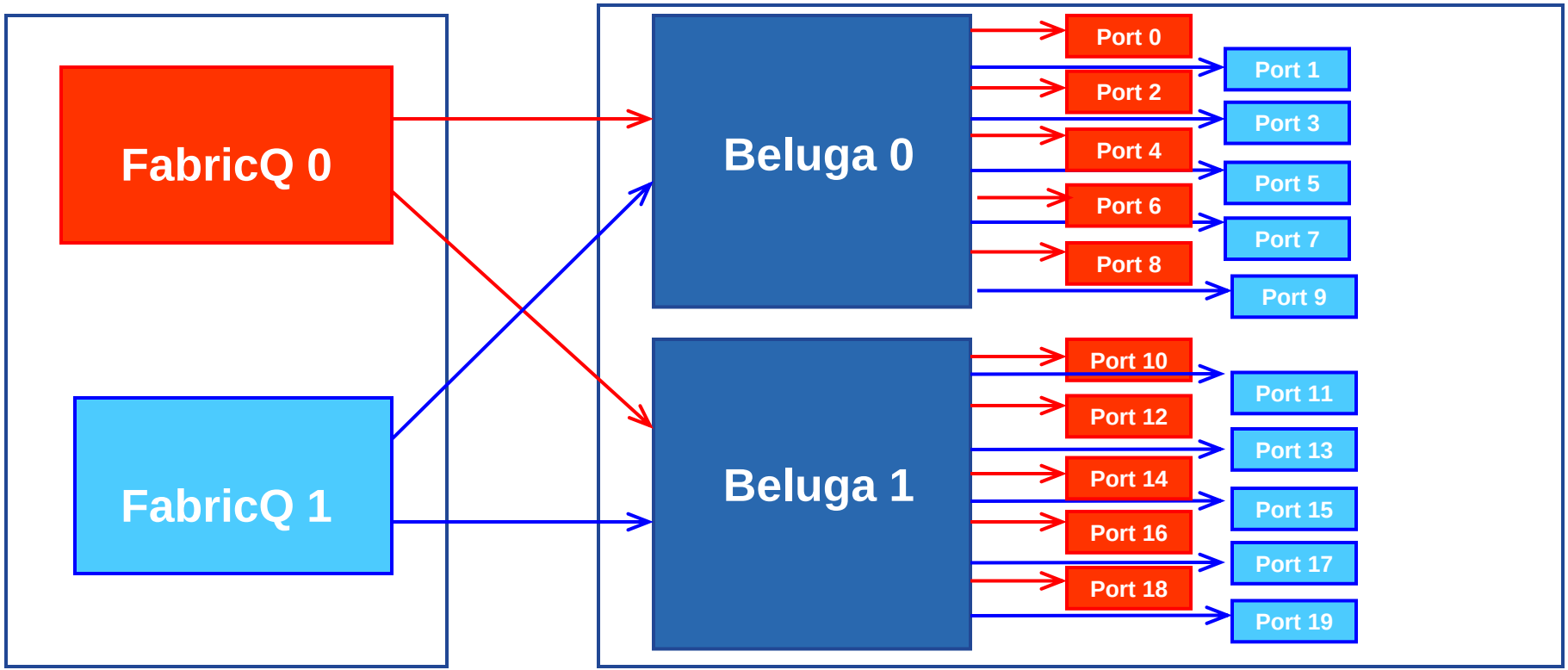




14x10GE Interface PLIM/FabricQ Mapping



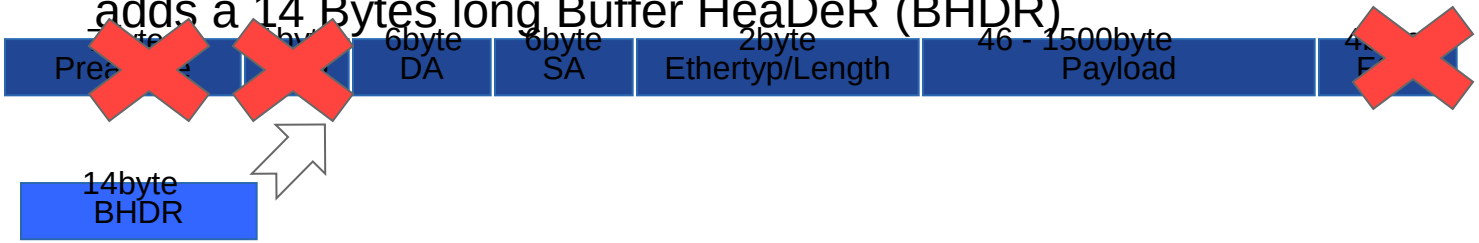
20x10GE Interface PLIM/FabricQ Mapping



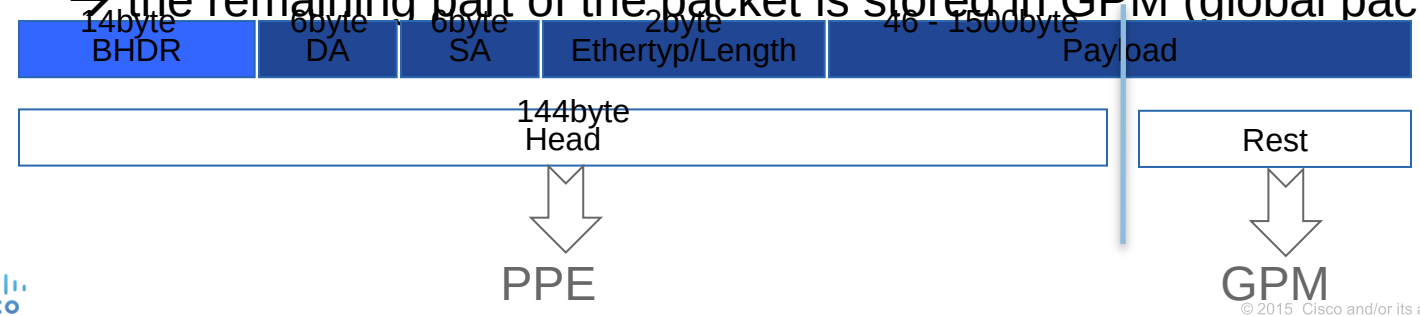
CRS-3 Life of a Packet

Life of a packet

- In the PLIM, Beluga
  removes FCS, preamble and flags from frame
  adds a 14 Bytes long Buffer HeaDeR (BHDR)

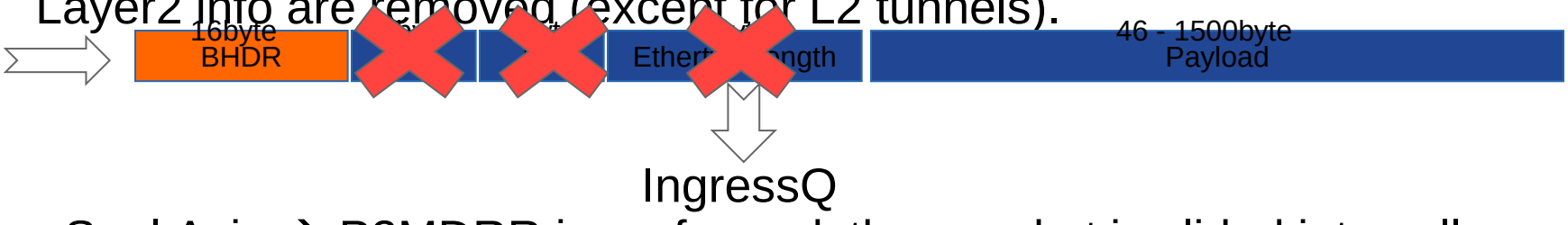


- This packet is passed to iPogo
  → stored in the PSE memory
  → first 144bytes (=head) are extract and passed to an available PPE
  → the remaining part of the packet is stored in GPM (global packet mem)

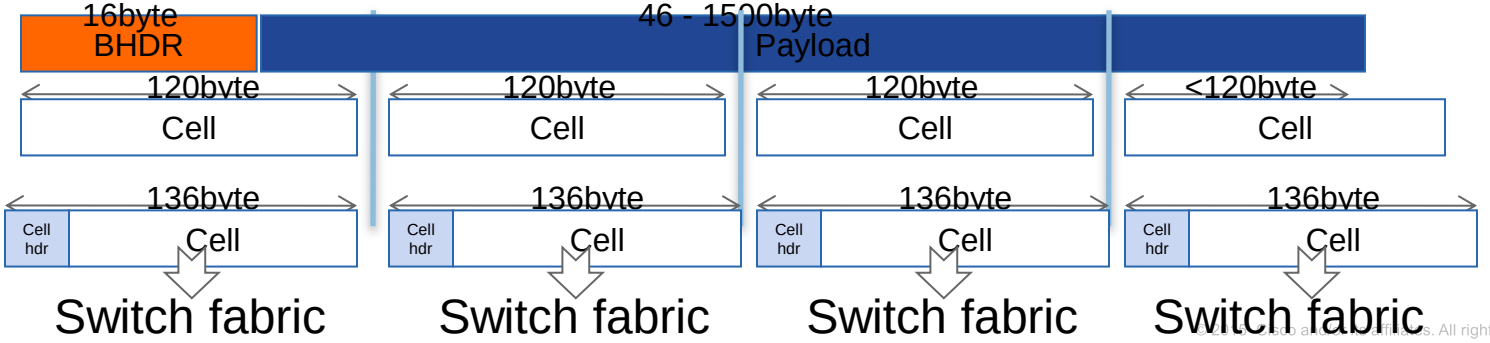


Life of a packet

- PPE performs destination lookup → slot and port
- Features are applied
- New BHDR (16B) is created, and BHDR+Head+Rest are recombined, Layer2 info are removed (except for L2 tunnels).

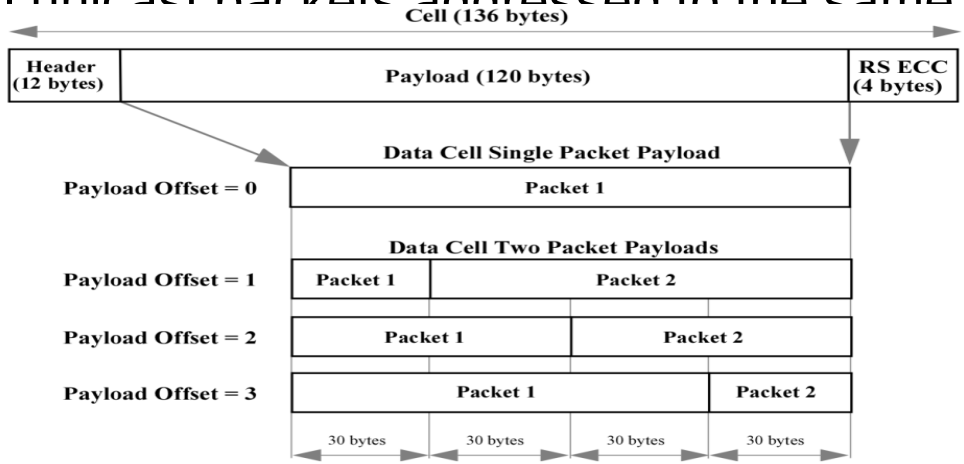


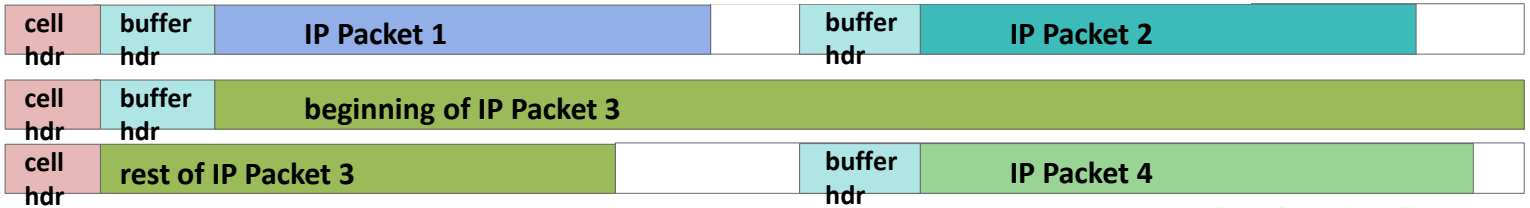
- Seal Asic → P2MDRR is performed, then packet is slided into cells.



Life of a packet

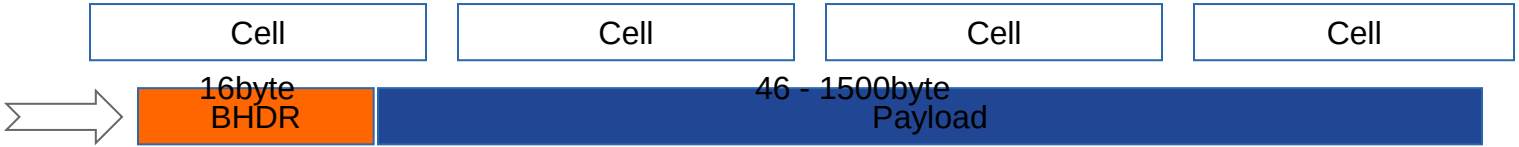
- Packet packing is possible on the CRS
- Packets are 136 byte, with a 120 bytes payload
- When small unicast packets addressed to the same destination arrive, then cell.



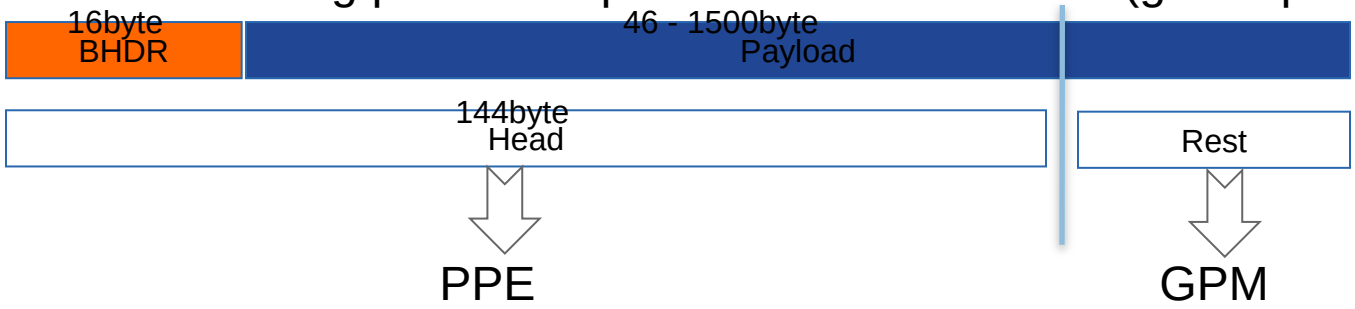


Life of a packet

- Cells from a given packets arrives on the same Crab ASIC (based on the destination port). Cells are buffered and packet is reassembled.

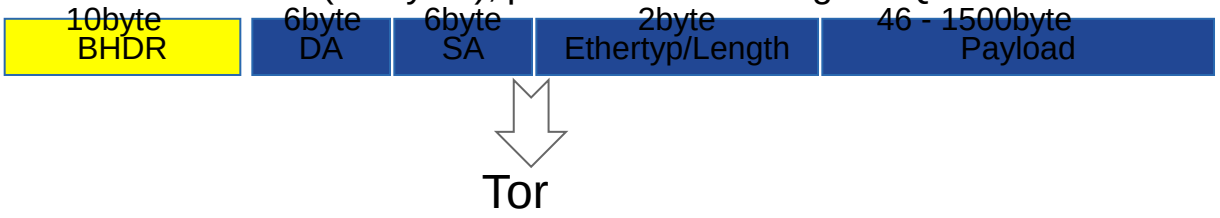


- Packet is queued before being sent to ePogo.
  → stored in the PSE memory
  → first 144bytes (=head) are extract and passed to an available PPE
  → the remaining part of the packet is stored in GPM (global packet mem)

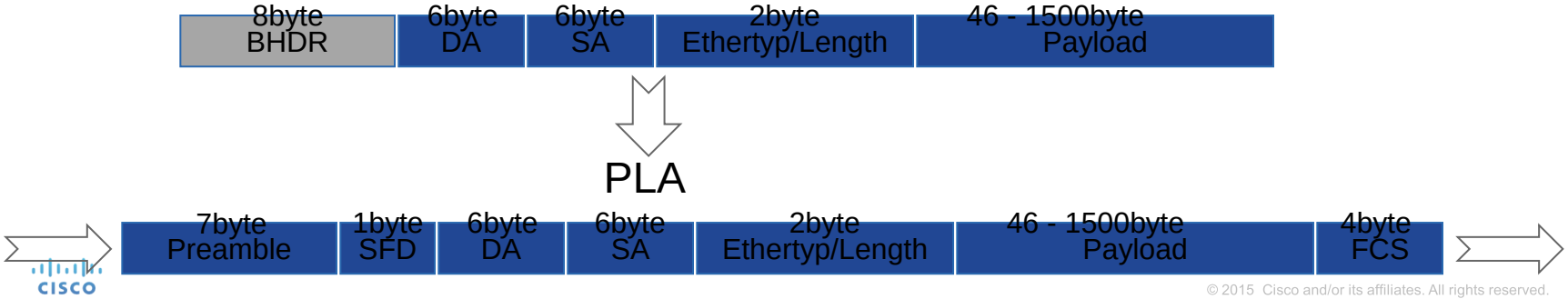


Life of a packet

- PPE performs destination lookup → L2 info is applied
- Features are applied (QoS, …)
- A new BHDR is created (10 bytes), packet is sent to EgressQ.

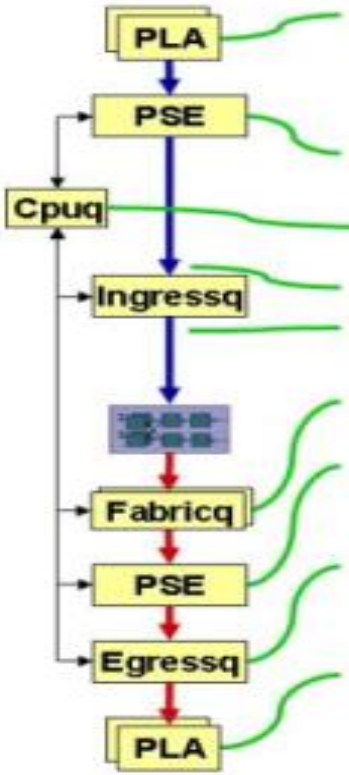


- In EgressQ ASIC, packet is queued before shaping and P2MDRR.
- Packet is then dequeued, a new 8 bytes BHDR is created, before passing to Beluga (PLA).



CRS-3 Troubleshooting

Flowchart for Troubleshooting Packet Drops



1. show interfaces [type] R/S/M
   show controllers plim asic statistics interface [type] R/S/M
   show controllers plim asic statistics summary location R/S/M
2. show controllers pse summary location R/S/M
   show controllers pse statistics ingress location R/S/M
   show controllers cpuctrl ports ingressq pdma queue all active loc R/S/M
3. show controller ingressq statistics location R/S/M
4. show controller ingressq statistics location R/S/M
5. show controllers fabricq statistics location R/S/M
6. show controllers pse summary location R/S/M
   show controllers pse statistics egress location R/S/M
7. show controllers egressq statistics location R/S/M
   show controllers egressq queue all location R/S/M
8. show controllers plim asic statistics interface R/S/M
   show controllers plim asic statistics summary location R/S/M
   show interfaces [type] R/S/M

PLIM Statistics - show interface

```
RP/0/RP0/CPU0:ROUTER#sh int te0/0/0/0
TenGigE0/0/0/0 is up, line protocol is up
  Interface state transitions: 7
  Hardware is TenGigE, address is 001f.ca03.a803 (bia 001f.ca03.ab29)
  Description: Vers LYO1-CRS-3/0.6.0.0/SFRI05773-05774
  Internet address is Unknown
  MTU 2014 bytes, BW 10000000 Kbit (Max: 10000000 Kbit)
     reliability 254/255, txload 73/255, rxload 11/255
  Encapsulation ARPA,
  Full-duplex, 10000Mb/s, LR, link type is force-up
  output flow control is off, input flow control is off
  loopback not set,
  ARP type ARPA, ARP timeout 04:00:00
  Last input 00:00:00, output 00:00:00
  Last clearing of "show interface" counters 6w0d
  30 second input rate 470429000 bits/sec, 153072 packets/sec
  30 second output rate 2871121000 bits/sec, 492251 packets/sec
     664031113796 packets input, 258120847544493 bytes, 0 total input drops
     0 drops for unrecognized upper-level protocol
     Received 0 broadcast packets, 2816363173 multicast packets
              0 runts, 0 giants, 0 throttles, 0 parity
     0 input errors, 0 CRC, 0 frame, 0 overrun, 0 ignored, 0 abort
     1642373738027 packets output, 1383779973854762 bytes, 0 total output drops
     Output 0 broadcast packets, 46968553705 multicast packets
     0 output errors, 0 underruns, 0 applique, 0 resets
     0 output buffer failures, 0 output buffers swapped out
     0 carrier transitions
```

show controllers

```
RP/0/RP0/CPU0:ROUTER#sh controllers tenGigE 0/0/0/0 bert
Command not supported on this interface
RP/0/RP0/CPU0:ROUTER#sh controllers tenGigE 0/0/0/0 internal

Total Power Available on PLIM for XFP's: 35000 mW
  Power used by Inserted XFP's: 21000 mW
  Power Available: 14000 mW

     Port          Power Used        State
      00            1500 mW          XFP Inserted and Powered On
      01            1500 mW          XFP Inserted and Powered On
      02            1500 mW          XFP Inserted and Powered On
      03            1500 mW          XFP Inserted and Powered On
      04            1500 mW          XFP Inserted and Powered On
      05            1500 mW          XFP Inserted and Powered On
      06            1500 mW          XFP Inserted and Powered On
      07            1500 mW          XFP Inserted and Powered On
      08            1500 mW          XFP Inserted and Powered On
      09            1500 mW          XFP Inserted and Powered On
      10            1500 mW          XFP Inserted and Powered On
      11            1500 mW          XFP Inserted and Powered On
      12            1500 mW          XFP Inserted and Powered On
      13            1500 mW          XFP Inserted and Powered On
```

Doesn't matter the port, it will display info for the slot.

show controllers tenGigE … phy (1/2)

```
RP/0/RP0/CPU0:ROUTER#sh contr tenGigE 0/0/0/0 phy

802.3ae Sections
================

PMA/PMD
  Previous Alarm Status:
    PMA/PMD Locked to Local Signal
    SR Ability
    Loopback Ability
  Current Alarm Status:
    PMA/PMD Locked to Local Signal
    SR Ability
    Loopback Ability

PCS
  Previous Alarm Status:
    PCS Rx Link UP
    PCS Rx Block Locked
    PCS Rx Link Status UP
    PCS Error'd Block Counts: 0
    PCS BER Counts: 0
    PCS has Block Lock
  Current Alarm Status:
    PCS Rx Link UP
    PCS Rx Block Locked
    PCS Rx Link Status UP
    PCS Error'd Block Counts: 0
    PCS BER Counts: 0
    PCS has Block Lock

WIS: HW In LAN Mode - No Info
...
```

```
XFP General Info:
=================

PHY/XFP Status:  XFP is Working as expected


XFP Info:
=========
Max Power Dissipation: 1500 mW

XFP Type: 10GBASE-LR
Vendor Name: CISCO-AVAGO
Vendor Part Number: SFCT-7081Z-CS2
Vendor OUI: 0x00-0x17-0x6a
Vendor Hardware Revision: 01
Vendor Serial number: AGA1450N9C8
Date Code (yy/mm/dd): 10/12/18
Lot Code: 01

Cisco PID: XFP10GLR-192SR-L
Cisco VID: V01
Cisco PN: 10-2542-01

ID: XFP
Extended ID: 0x18
  TX ref clock input is not required
  CDP is supported
  Power Level 1 (1.5W max. power)
Minimum bit rate is 9900 MBits/s.
Maximum bit rate is 11100 MBits/s.
...
```

Non Cisco XFP: “XFP Not UDI Compliant”

show controllers tenGigE … phy (2/2)

```
XFP Detail Info:
================
Temp: 26.234
Tx bias: 33.630 mA
Tx power: 0.5186 mW ( -2.9 dBm)
Rx power: 0.3916 mW ( -4.1 dBm)
AUX 1: Laser Temperature: 0x40
AUX 2: +3.3V Supply Voltage: 0x7

XFP Status: enabled.
 laser is enabled
 MOD NR is ready
 is powered on
 has interrupt(s)
 has no LOS
 data is ready
 TX path is ready
 TX laser is not in fault condition
 TX path CDR is locked
 RX path is ready
 RX path CDR is locked

Alarms: No active alarms

Warnings: No active warning

THRESHOLDS
                          High Alarm      Low Alarm      High Warning      Low Warning
   Temperature      C         78.0            0.0             73.0             5.0
   Voltage          V      000.0000        000.0000        000.0000         000.0000
   Bias Current     mA     090.0000        005.0000        075.0000         015.0000
   Transmit power   mW     022.3870        000.7580        011.2200         001.5130
   Receive power    mW     022.3870        000.1810        011.2200         000.3630
```

show controllers plim asic (1/3)

```
RP/0/RP0/CPU0:ROUTER#sh controllers plim asic statistics interface te0/0/0/0
Node: 0/0/CPU0
------------------------------------------------------------------------------
TenGigE0/0/0/0 Tx Statistics
------------------------------------------------
Total Packets              : 3297180649474     Total Bytes                : 2760010567839284
Total Good Packets         : 3297180649477     Total Good Bytes           : 2760010567842366
Unicast Packets            : 3198084897557     Multicast Packets          : 99095751930
Broadcast Packets          : 1                 64 Byte Packets            : 3313264
65to127  Byte Packets      : 711438222235      128to257 Byte Packets      : 796987491277
256to511 Byte Packets      : 71707627508       512to1023 Byte Packets     : 74691011513
1024to1518 Byte Packets    : 1309370894470     1519to1522 Byte Packets    : 7557542944
1523to1548 Byte Packets    : 310314218341      1549to2000 Byte Packets    : 15108013317
2001to_MRU Byte Packets    : 2314617           Non Pause BPDU Packets     : 0
Classic Pause Packets      : 0                 Shaped Pause Packets       : 0
Class Based Pause Pkts 0   : 0                 Class Based Pause Pkts 1   : 0
Class Based Pause Pkts 2   : 0                 Class Based Pause Pkts 3   : 0
Class Based Pause Pkts 4   : 0                 Class Based Pause Pkts 5   : 0
Class Based Pause Pkts 6   : 0                 Class Based Pause Pkts 7   : 0
Dropped Packets
===============
Drained Packets            : 1                 Abort                      : 0
Length Error               : 0                 Giant                      : 0
Tail Drop: HP Queue        : 0                 Tail Drop: LP Queue        : 0

...
```

If Pause frame is configured

If CB Pause frame is configured

show controllers plim asic (2/3)

```
...

TenGigE0/0/0/0 Rx Statistics
-------------------------------------------
Total Packets              : 1333474090155     Total Bytes                : 535804418768609
Total Good Packets         : 1333474090158     Total Good Bytes           : 535804418771230
Unicast Packets            : 1327152179475     Multicast Packets          : 6321910682
Broadcast Packets          : 1                 64 Byte Packets            : 11073341
65to127  Byte Packets      : 732873834933      128to257 Byte Packets      : 267718629405
256to511 Byte Packets      : 31771535618       512to1023 Byte Packets     : 42353929858
1024to1518 Byte Packets    : 187975360954      1519to1522 Byte Packets    : 1178135139
1523to1548 Byte Packets    : 64271466724       1549to2000 Byte Packets    : 5319070020
2001to_MRU Byte Packets    : 1054166           Non Pause BPDU Packets     : 0
Classic Pause Packets      : 0
Class Based Pause Pkts 0   : 0                 Class Based Pause Pkts 1   : 0
Class Based Pause Pkts 2   : 0                 Class Based Pause Pkts 3   : 0
Class Based Pause Pkts 4   : 0                 Class Based Pause Pkts 5   : 0
Class Based Pause Pkts 6   : 0                 Class Based Pause Pkts 7   : 0

...
```

show controllers plim asic (3/3)

```
...

Dropped Packets
===============
Runts                          : 0          Fragments                      : 0
Jumbo                          : 0          Jabber                         : 0
CRC                            : 0          Code Error                     : 0
Code Violation                 : 290        Bad Preamble                   : 0
IPG Violation                  : 0
Packet HPQ QoS Ctl Drop        : 0          Bytes HPQ QoS Ctl Drop         : 0
Packet HPQ QoS HP Drop         : 0          Bytes HPQ QoS HP Drop          : 0
Packet HPQ Ctl Tail Drop       : 0          Bytes HPQ Ctl Tail Drop        : 0
Packet HPQ HP Tail Drop        : 0          Bytes HPQ HP Tail Drop         : 0
Packet LPQ LP1 Tail Drop       : 0          Bytes LPQ LP1 Tail Drop        : 0
Packet LPQ LP2 Tail Drop       : 0          Bytes LPQ LP2 Tail Drop        : 0
Packet TCAM Miss               : 0          Bytes TCAM Miss                : 0
Packet EOP Abort Drop          : 0          Bytes EOP Abort Drop           : 0
Packet Policy Deny             : 0          Bytes Policy Deny              : 0

Rx Packet Drop Details
======================
Unknown Dest MAC Pkts          : 1267853
Unknown E-Type Pkts            : 0
Unknown Encap Pkts             : 0          Unknown Encap Bytes            : 0
Unknown VLAN Pkts              : 0          Unknown VLAN Bytes             : 0
```

QoS PLIM dropped packets won't appear in "sh policy-map interface" but here.

show controllers plim asic stat …

```
RP/0/RP0/CPU0:ROUTER#sh contr plim asic stat sum loc 0/0/CPU0

                          Node: 0/0/CPU0
------------------------------------------------------------------
Instance# 0 Statistics
----------------------------------------
To PSE   : Total Good Packets          : 8832378239403
To PSE   : Total Good Bytes            : 4237198815950608
To PSE   : Total Errored Packets       : 0
From TxIlite: Total Hard BP Count      : 356471049
From PSE: Total Low Priority BP Count: 356471051
From EgressQ: Total Good Packets       : 17074922265855
From EgressQ: Total Good Bytes         : 13338280868103881
From EgressQ: Total Errored Packets    : 0
From EgressQ: Pkts:Invalid Interface   : 0

Instance# 1 Statistics
----------------------------------------
To PSE   : Total Good Packets          : 4812355409772
To PSE   : Total Good Bytes            : 3165474187759645
To PSE   : Total Errored Packets       : 0
From TxIlite: Total Hard BP Count      : 327693943
From PSE: Total Low Priority BP Count: 327693945
From EgressQ: Total Good Packets       : 7385562122265
From EgressQ: Total Good Bytes         : 5862349866242030
From EgressQ: Total Errored Packets    : 0
From EgressQ: Pkts:Invalid Interface   : 0
```

Number of 312.5MHz clock cycles during which hard back pressure has been asserted to the ASIC core by the I-lite TX.

show controllers c2c … (1/2)

```
RP/0/RP0/CPU0:ROUTER#sh contr c2c PLIM-ASIC_0 links all loc 0/0/CPU0

C2C links:
--------------------------------------------------------------------------
ASIC Id         Peer Id         Type   Link-Id    State
--------------------------------------------------------------------------
PLIM-ASIC_0     EGRESSQ_0         RX   0xe01      Up
PSE_0           PLIM-ASIC_0       TX   0x105      Up
RP/0/RP0/CPU0:ROUTER#
RP/0/RP0/CPU0:ROUTER#sh contr c2c PLIM-ASIC_1 links all loc 0/0/CPU0

C2C links:
--------------------------------------------------------------------------
ASIC Id         Peer Id         Type   Link-Id    State
--------------------------------------------------------------------------
PLIM-ASIC_1     EGRESSQ_0         RX   0xe02      Up
PSE_0           PLIM-ASIC_1       TX   0x205      Up
```

show controllers c2c … (2/2)

```
RP/0/RP0/CPU0:ROUTER#sh contr c2c PLIM-ASIC_0 links all hw info location 0/0/CPU0

    I-lite link information for link ID 0x00000e01
      Internal info:
        Bandwidth:     80 Gbps
        Status:        Up
        Enabled:       Datapath - Yes, Return Bus - Yes
        Flags:         0x00000004
        fc_to_send:    0x00000016
        Debug level:   0x00000000
      ASIC regs:
        Link enable:                0x00000003
        Link err intr enable:       0x00001fff
        Link nonerr intr enable:    0x00000006
        RB config:                  0x00000161
        RB status:                  0x00000020

    I-lite link information for link ID 0x00000105
      Internal info:
        Bandwidth:     100 Gbps
        Status:        Up
        BP threshold:  0
        Enabled:       Datapath - Yes, Return Bus - Yes
        Flags:         0x00000000
        Debug level:   0x00000000
      ASIC regs:
        Link enable:                0x00000003
        Link err intr enable:       0x000007ff
        RB config:                  0x00000000
        RB status:                  0x00000201
        RB err intr enable:         0x000003e3
        RB nonerr intr enable:      0x0000001e
```

PLIM-ASIC_0 → EGRESSQ_0

PSE_0 → PLIM-ASIC_0

show controllers pse sum / CRS-3

```
RP/0/RP0/CPU0:ROUTER#show controllers pse summary location 0/0/CPU0

              Node: 0/0/CPU0:
-------------------------------------------------

Ingress PSE, Summary Info:
-------------------------------------------------
IBM P/N      : 36         LotNum       : 818
SerialNum    : 00000000   BadPPECls1   : 0x04 : 0x01
BadPPECls2   : 0000 : 0x02
Version      : 2          CpuctrlPort  : 0
DeviceState  : 128 (INIT_COMPLETE and OPERATIONAL)
StartupOpts  : 00000000   MmappedBase  : 00000000
ClsDisMask   : 0x241      NFusedPPEs   : 0    (0 hwf, 0 swf)
MPUcodeName  : /pkg/ucode/crs/pse/pogo_ingress_mp_v2.mucode
PPEUcodeName: /pkg/ucode/crs/pse/pogo_ingress_turbo_ether_v1.mucode
INTR-Status  : 00000000   INTR-Enable  : 0x1ffffff
NHardResets  : 0          NPonResets   : 0
NPPEUcDlds   : 0          NResetRetry  : 0
NIntrtps     : 0          NIntrptThrot: 0

...
```

"128 (INIT_COMPLETE and OPERATIONAL)" is a normal state

show controllers pse statistics

```
RP/0/RP0/CPU0:ROUTER#show contr pse statistics location 0/0/CPU0

Node 0/0/CPU0 Ingress PSE Stats
--------------------------------

Punt Stats                                Punted          Policed & Dropped
----------                                ------          -----------------
CDP                                       1506941         0
ARP                                       2354            0
Bundle Control                            2735530         0
IPv4 options                              104533          1
IPv4 TTL expiration                       595843          546527
IPv4 L2LI punt                            68245           0
IPv4 MC do all                            1428264         451164
IPv4 MC do all but forward                6366263         1716346
MPLS TTL expiration, IP payload           56127           400477

Drop Stats                                Dropped
----------                                -------
L2 unknown                                7398043
IFIB policer drop                         756
Drop due to bad queue limit               1792
IPv4 not enabled                          1
IPv4 interface down                       15760
IPv4 addr sanity                          3299
IPv4 length error                         8
IPv4 L2LI drop                            68869
...
```

Will not show counters at zero.
→ Use option “all” for a full display.

```
...
IPv4 MC unexpected input interface        5822333
IPv6 not enabled                          3818
MPLS interface down                       45089
MPLS PLU no match                         9559405
MPLS L2LI drop                            1712739

Debug Stats                               Count
-----------                               -----
No non-zero Debug Stats
```

PPE idle counter is at 0 on Pogo

show controllers c2c …

```
RP/0/RP0/CPU0:ROUTER#sh contr c2c PSE_0 links all loc 0/0/CPU0

C2C links:
--------------------------------------------------------------------------
ASIC Id         Peer Id         Type   Link-Id    State
--------------------------------------------------------------------------
PSE_0           PLIM-ASIC_0      RX    0x105      Up
PSE_0           PLIM-ASIC_1      RX    0x10205    Up
INGRESSQ_0      PSE_0            TX    0x507      Up

RP/0/RP0/CPU0:ROUTER#sh contr c2c PSE_0 links all hw info loc 0/0/CPU0

    I-lite link information for link ID 0x00000105
      Internal info:
        Bandwidth:     100 Gbps
        Status:        Up
        Enabled:       Datapath - Yes, Return Bus - Yes
        Flags:         0x00000006
        fc_to_send:    0x00000001
        Debug level:   0x00000000
      ASIC regs:
        Link enable:                0x00000033
        Link err intr enable:       0x00001fff
        Link nonerr intr enable:    0x00000006
        RB config:                  0x00000011
        RB status:                  0x00000020

    ...
```

PLIM-ASIC_0 → PSE_0

show controllers c2c …

```
...  I-lite link information for link ID 0x00010205
       Internal info:
         Bandwidth:     100 Gbps
         Status:        Up
         Enabled:       Datapath - Yes, Return Bus - Yes
         Flags:         0x00000006
         fc_to_send:    0x00000001
         Debug level:   0x00000000
       ASIC regs:
         Link enable:                0x00000033
         Link err intr enable:       0x00001fff
         Link nonerr intr enable:    0x00000000
         RB config:                  0x00000011
         RB status:                  0x00000020

     I-lite link information for link ID 0x00000507
       Internal info:
         Bandwidth:     160 Gbps
         Status:        Up
         BP threshold:  0
         Enabled:       Datapath - Yes, Return Bus - Yes
         Flags:         0x00000000
         Debug level:   0x00000000
       ASIC regs:
         Link enable:                0x00000003
         Link err intr enable:       0x00000fff
         RB config:                  0x00000000
         RB status:                  0x00000801
         RB err intr enable:         0x000001e3
         RB nonerr intr enable:      0x0000001e
```

PLIM-ASIC_1 → PSE_0

PSE_0 → INGRESSQ_0

show controllers pse stats

```
RP/0/RP0/CPU0:CRS-F#show controllers pse statistics location 0/1/CPU0
Node 0/1/CPU0 Ingress PSE Stats
------------------------------
Punt Stats                      Punted        Policed & Dropped
----------                      ------        -----------------
L2 control                           3                    0
ARP              190     0
IPv4 PLU no match                536567       7443303015       <<<< Packets with no route >>>>
IPv4 TTL expiration              362298       1236786496941

Drop Stats                      Dropped
----------                      -------
IPv4 checksum error              76634126
IPv4 addr sanity                 4649539181              <<<< IPv4 sanity check failed >>>>

Debug Stats                     Count
-----------                     -----
PPE idle counter                829984169

RP/0/RP0/CPU0:CRS-1#sh controllers pse stat ingress location 0/1/cpu0 | i checksum
IPv4 checksum error              997378265
RP/0/RP0/CPU0:CRS-10#sh controllers pse stat ingress location 0/1/cpu0 | i checksum
IPv4 checksum error              1033084922

RP/0/RP0/CPU0:CRS-1#sh ipv4 traffic
 IP statistics:
  Rcvd:  19157762 total, 252754 local destination
         0 format errors, 0 bad hop count
         56080 unknown protocol, 0 not a gateway
         0 security failures, 0 bad source, 2761423364 bad header        <<<< This is aggregate for all LCs >>>>>
         0 with options, 0 bad, 0 unknown
  Opts:  0 end, 0 nop, 0 basic security, 0 extended security
```

show controllers ingressq sum

```
RP/0/RP0/CPU0:ROUTER#sh contr ingressq summary location 0/0/CPU0
ASIC State
----------
Asic Type                Seal rev 3
IQM number               2
Halted                   False
Interrupt Status         0x0
Interrupt Enable         0x7fffffff        [Expected: 0x7fffffff]
Force HPI BP             False
Force Pogo BP            False
Sequencer state:         SEAL_SEQ_ST_IDLE [Expected: SEAL_SEQ_ST_IDLE]
--------
Barriers
--------
Cast/Pri                 t0                t1                Duration(usec)
Unicast High          0xafeac853c3         0xafeac9d9bb              10
Unicast Low           0xb0336ba3d7         0xb0336d2a81              9
Multicast High        0xb13ef631a7         0xb13ef7ba7e              9
Multicast Low         0xb1b0b91598         0xb1b0ba9f4c              9
----------
Link State
----------
To Fabric:
          TFI Physical link mask:              0xffffffffff [Max links: 48]
          TFI Virtual  link mask:              0xffffffffff [Max links: 40]
          LNS Virtual links per plane 0:       0x1f
          LNS Virtual links per plane 1:       0x1f
...
```

Repeat command twice and verify barriers counters increase

show controllers ingressq statistics

```
RP/0/RP0/CPU0:ROUTER#show controllers ingressq statistics location 0/0/CPU0
Ingressq Rx Statistics.
------------------------------------------------------------------------
rx pkts                          :   13016639280590 (6854625053013142 bytes)
rx pkts from cpu                 :         38224901 (     26281695184 bytes)
rx pkts from pse                 :   13016601055689 (6854598771317958 bytes)

HPI Pkts Statistics
------------------------------------------------------------------------
HPI to cpu pkts                  :        217447088 (    403208841853 bytes)
HPI from cpu pkts                :         38224901 (     25822996372 bytes)

Ingressq Tx Statistics
------------------------------------------------------------------------
tx cells to fabric               :   61199854150515
unicast low priority cells       :   46986297689020
unicast high priority cells      :    4654508595968
multicast low priority cells     :    9559047864953
multicast high priority cells    :             574
```

New in Seal:
Host Processor Interface (HPI) → connects Seal to MSC CPU on Kensho

show controllers ingressq statistics

```
...
Ingressq Drops.
------------------------------------------------------------------------
length error drops - PSE       :                0
giant pkt drops - Cpu          :                0
stomp packet drops - PSE       :                0
error pkt drops - Cpu          :                0
invalid destQ drops - PSE      :                0
invalid destQ drops - Cpu      :                0
destQ disabled drops - PSE     :                0
destQ disabled drops - Cpu     :               50
shapeQ disabled drops - PSE    :                0
shapeQ disabled drops - Cpu    :                0
discard drops                  :                0 (                0 bytes)
tail drops                     :                0 (                0 bytes)
mcl tail drops                 :                0 (                0 tridecs)
mch tail drops                 :                0 (                0 tridecs)
cells Drops                    :                0
ECC error drops                :                0
HPI down drops                 :                0 (                0 bytes)

Out of Resources Drops.
------------------------------------------------------------------------
OOR error drops - PSE          :                0 (                0 tridecs)
OOR error drops - Cpu          :                0 (                0 bytes)

Drain Drops.
------------------------------------------------------------------------
Fabric drops                   :                0
To-Cpu drops                   :                0 (                0 bytes)
```

More drop counters available in Seal than in Sprayer

show controllers c2c

```
RP/0/RP0/CPU0:ROUTER#sh contr c2c INGRESSQ_0 links all loc 0/0/CPU0

C2C links:
--------------------------------------------------------------------
ASIC Id        Peer Id        Type  Link-Id    State
--------------------------------------------------------------------
INGRESSQ_0     PSE_0            RX  0x507      Up

RP/0/RP0/CPU0:ROUTER#sh contr c2c INGRESSQ_0 links all hw info loc 0/0/CPU0

    I-lite link information for link ID 0x00000507
      Internal info:
        Bandwidth:     160 Gbps
        Status:        Up
        Enabled:       Datapath - Yes, Return Bus - Yes
        Flags:         0x00000002
        Debug level:   0x00000000
      ASIC regs:
        Link enable:                0x00000003
        Link err intr enable:       0x00000fff
        Link nonerr intr enable:    0x00000006
        RB config:                  0x00000001
        RB status:                  0x00000080
```

PSE_0 → INGRESSQ_0

32 iLite links @5Gbps from iPSE

160Gbps raw bw, 148Gbps for large packets

MSC140 – CRS-3 Fabric (8 slots)

```
RP/0/RP0/CPU0:ROUTER#sh contr ingressq fabric links loc 0/0/CPU0
Ingressq link state
plane-id    link-id     ADMIN-STATE OPER-STATE  AVAIL-STATE UP-COUNT
-------------------------------------------------------------.
0           0           UP          UP          UP          2
0           8           UP          UP          UP          2
0           16          UP          UP          UP          2
0           24          UP          UP          UP          2
0           32          UP          UP          UP          2
0           40          DOWN        DOWN        DOWN        0
1           1           UP          UP          UP          2
1           9           UP          UP          UP          2
1           17          UP          UP          UP          2
1           25          UP          UP          UP          2
1           33          UP          UP          UP          2
1           41          DOWN        DOWN        DOWN        0
2           2           UP          UP          UP          2
2           10          UP          UP          UP          2
2           18          UP          UP          UP          2
2           26          UP          UP          UP          2
2           34          UP          UP          UP          2
2           42          DOWN        DOWN        DOWN        0
3           3           UP          UP          UP          2
3           11          UP          UP          UP          2
3           19          UP          UP          UP          2
3           27          UP          UP          UP          2
3           35          UP          UP          UP          2
3           43          DOWN        DOWN        DOWN        0
4           4           UP          UP          UP          2
4           12          UP          UP          UP          2
4           20          UP          UP          UP          2
4           28          UP          UP          UP          2
4           36          UP          UP          UP          2
4           44          DOWN        DOWN        DOWN        0
...
```

8 slots → 1 link on 6 per plane is down

```
Ingressq link state
plane-id    link-id     ADMIN-STATE OPER-STATE  AVAIL-STATE UP
-------------------------------------------------------------.
...
5           5           UP          UP          UP          2
5           13          UP          UP          UP          2
5           21          UP          UP          UP          2
5           29          UP          UP          UP          2
5           37          UP          UP          UP          2
5           45          DOWN        DOWN        DOWN        0
6           6           UP          UP          UP          2
6           14          UP          UP          UP          2
6           22          UP          UP          UP          2
6           30          UP          UP          UP          2
6           38          UP          UP          UP          2
6           46          DOWN        DOWN        DOWN        0
7           7           UP          UP          UP          2
7           15          UP          UP          UP          2
7           23          UP          UP          UP          2
7           31          UP          UP          UP          2
7           39          UP          UP          UP          2
7           47          DOWN        DOWN        DOWN        0
-------------------------------------------------------------.
RP/0/RP0/CPU0:ROUTER#
```

48 LR SERDES lanes @5Gbps to fabric

40 used for 200Gbps raw BW / 141 Gbps net BW

MSC-140 – CRS-3 Fabric (16 slots)

```
RP/0/RP0/CPU0:ROUTER#sh contr ingressq fabric links loc 0/14/CPU0
Ingressq link state
plane-id    link-id     ADMIN-STATE OPER-STATE  AVAIL-STATE UP-COUNT
-----------------------------------------------------------.
0           0           UP          UP          UP          2
0           8           UP          UP          UP          2
0           16          UP          UP          UP          2
0           24          UP          UP          UP          2
0           32          UP          UP          UP          2
0           40          UP          UP          UP          2
1           1           UP          UP          UP          2
1           9           UP          UP          UP          2
1           17          UP          UP          UP          2
1           25          UP          UP          UP          2
1           33          UP          UP          UP          2
1           41          UP          UP          UP          2
2           2           UP          UP          UP          2
2           10          UP          UP          UP          2
2           18          UP          UP          UP          2
2           26          UP          UP          UP          2
2           34          UP          UP          UP          2
2           42          UP          UP          UP          2
3           3           UP          UP          UP          2
3           11          UP          UP          UP          2
3           19          UP          UP          UP          2
3           27          UP          UP          UP          2
3           35          UP          UP          UP          2
3           43          UP          UP          UP          2
4           4           UP          UP          UP          2
4           12          UP          UP          UP          2
4           20          UP          UP          UP          2
4           28          UP          UP          UP          2
4           36          UP          UP          UP          2
4           44          UP          UP          UP          2
...
```

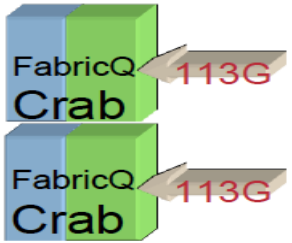
16 slots: all links up but rate limited to 5x5Gbps per plane

```
Ingressq link state
plane-id    link-id     ADMIN-STATE OPER-STATE  AVAIL-STATE UP
-----------------------------------------------------------.
...
5           5           UP          UP          UP          2
5           13          UP          UP          UP          2
5           21          UP          UP          UP          2
5           29          UP          UP          UP          2
5           37          UP          UP          UP          2
5           45          UP          UP          UP          2
6           6           UP          UP          UP          2
6           14          UP          UP          UP          2
6           22          UP          UP          UP          2
6           30          UP          UP          UP          2
6           38          UP          UP          UP          2
6           46          UP          UP          UP          2
7           7           UP          UP          UP          2
7           15          UP          UP          UP          2
7           23          UP          UP          UP          2
7           31          UP          UP          UP          2
7           39          UP          UP          UP          2
7           47          UP          UP          UP          2
-----------------------------------------------------------.
RP/0/RP0/CPU0:ROUTER#
```

48 LR SERDES lanes @5Gbps to fabric
rate limited to 200Gbps raw BW / 141 Gbps net BW

show contr fabricq sum

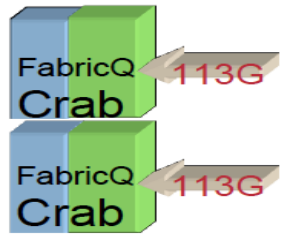
```
RP/0/RP0/CPU0:ROUTER#sh contr fabricq summary location 0/0/CPU0

 Fabricq Generic Details:
  Card:        MSC          Node-id: 0/0/CPU0 (0x1)
  Profile Filename:  fqm_driver_profiles.prof    Link Retry Period: 0
  Driver Flags:
  Cpuctrl DMA Init done: 1     Gaspp Init done: 1
  Fabric Init required: 0
  Asic Details:
  Asic State:  1
  Asic Id:          2f00000001216088c8e82403e3210240    Cpuctrl device Number:  0
  Asic Revision:    2
  Asic Instance:    0     Fabric Destination Address:  0
  Cpuctrl net port:          0
  PCI Base:          0xf00000000    Mmaped PCI Base:     0x0
  ASIC Instance Flags:
  RLDRAM Bist Done: 0    Other Bist done:    0
  Cpuctrl Init done:     1    Module Inits done:  1
  Barrier synced on 32 links
  I-lite link status: Link up
  Block init state: All blocks initialized
  Block halt state: None halted
  +-------------------------------------------------------------------------+
← ...snip...same kind of output for ASIC instance 1...snip... →
```



32 links from the fabric synced

show contr fabricq link-info

```
RP/0/RP0/CPU0:ROUTER#sh contr fabricq link-info all loc 0/0/CPU0

  Location:  0/0/CPU0
  Asic Instance:   0
  Fabric Destination Address:     0
  Retry period:  0 sec
  Link Active bitmap (1=up,0=down):  0xffffffff
  +-------------------------------------------------------------------------+
  |Link #|Driver state | FSDB state  |Barrier state|Up (Drv Barr)| Errors  |
  +-------------------------------------------------------------------------+
  |    0 |      Up     |      Up     |      Up     |      1   1  |         |
  |    1 |      Up     |      Up     |      Up     |      1   1  |         |
  |    2 |      Up     |      Up     |      Up     |      1   1  |         |
  |    3 |      Up     |      Up     |      Up     |      1   1  |         |
  |    4 |      Up     |      Up     |      Up     |      1   1  |         |
  |    5 |      Up     |      Up     |      Up     |      1   1  |         |
  |    6 |      Up     |      Up     |      Up     |      1   1  |         |
...
  |   24 |      Up     |      Up     |      Up     |      1   1  |         |
  |   25 |      Up     |      Up     |      Up     |      1   1  |         |
  |   26 |      Up     |      Up     |      Up     |      1   1  |         |
  |   27 |      Up     |      Up     |      Up     |      1   1  |         |
  |   28 |      Up     |      Up     |      Up     |      1   1  |         |
  |   29 |      Up     |      Up     |      Up     |      1   1  |         |
  |   30 |      Up     |      Up     |      Up     |      1   1  |         |
  |   31 |      Up     |      Up     |      Up     |      1   1  |         |
  +-------------------------------------------------------------------------+
```

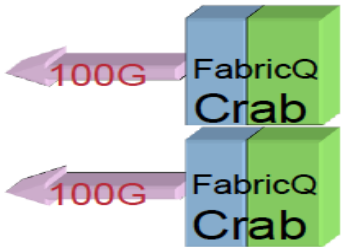


32 links up / No errors

show contr c2c FABRICQ_0 links

```
RP/0/RP0/CPU0:ROUTER#sh contr c2c FABRICQ_0 links all loc 0/0/CPU0

C2C links:
--------------------------------------------------------------------------
ASIC Id         Peer Id         Type  Link-Id    State
--------------------------------------------------------------------------
PSE_1           FABRICQ_0         TX  0xa06      Up

RP/0/RP0/CPU0:ROUTER#sh contr c2c FABRICQ_0 links all hw info loc 0/0/CPU0

    I-lite link information for link ID 0x00000a06
      Internal info:
        Bandwidth:     100 Gbps
        Status:        Up
        BP threshold:  0
        Enabled:       Datapath - Yes, Return Bus - Yes
        Flags:         0x00000000
        Debug level:   0x00000000
      ASIC regs:
        Link enable:                0x00000003
        Link err intr enable:       0x00000fff
        RB config:                  0x00000000
        RB status:                  0x00000201
        RB err intr enable:         0x000003e3
        RB nonerr intr enable:      0x0000001e
```

FABRICQ_0 → PSE_1



show contr fabricq link-info

```
RP/0/RP0/CPU0:ROUTER#show contr fabricq statistics loc 0/0/CPU0

  Fabric Queue Manager Packet Statistics
  ======================================

  Location: 0/0/CPU0
  Asic Instance: 0
  Fabric Destination Address: 0
  BP Asserted Count     :    77343684649679 (+   77343684649679 )
  MC BP Asserted Count  :                 0 (+                0 )

  Input Cell counters:
  +-------------------------------------------------------------+
  Data cells            :    94122772749140 (+   94122772749140 )
  Control cells         :       29310485780 (+      29310485780 )
  Idle    cells         :   790213267186562 (+ 790213267186562 )

  Reassembled packet counters
  +-------------------------------------------------------------+
  Ucast pkts            :    13316517905146 (+   13316517905146 )
  Mcast pkts            :      280349571670 (+     280349571670 )
  Cpuctrlcast pkts      :         144047784 (+        144047784 )

  Dropped packets
  +-------------------------------------------------------------+
  Ucast pkts            :             65626 (+             65626 )
  Mcast pkts            :                 0 (+                 0 )
  Cpuctrlcast pkts      :                 0 (+                 0 )
  Vital denied pkts     :                 0 (+                 0 )
  NonVital denied pkts  :                 0 (+                 0 )
  Unicast lost pkts     :             16392 (+             16392 )
  Ucast partial pkts    :           1079315 (+           1079315 )
  PSM OOR Drops         :                 0 (+                 0 )
...
```

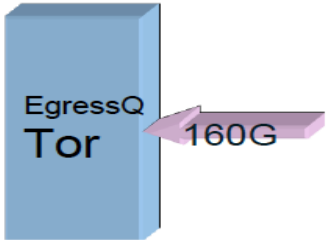
Address used by IngressQ to send cell to a particular Crab. Each Crab is assigned a unique address when initialized.

Vital are HP packets

All drops should be checked…

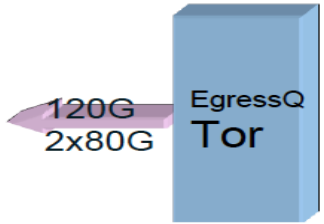
show contr c2c EGRESSQ_0 links all

```
RP/0/RP0/CPU0:ROUTER#sh contr c2c EGRESSQ_0 links all loc 0/0/CPU0

C2C links:
--------------------------------------------------------------------
ASIC Id         Peer Id         Type  Link-Id    State
--------------------------------------------------------------------
EGRESSQ_0       PSE_1             RX  0x60e      Up
PLIM-ASIC_0     EGRESSQ_0         TX  0xe01      Up
PLIM-ASIC_1     EGRESSQ_0         TX  0x10e02    Up

RP/0/RP0/CPU0:ROUTER#sh contr c2c EGRESSQ_0 links all hw info loc 0/0/CPU0

    I-lite link information for link ID 0x0000060e
      Internal info:
        Bandwidth:     160 Gbps
        Status:        Up
        Enabled:       Datapath - Yes, Return Bus - Yes
        Flags:         0x00000002
        Debug level:   0x00000000
      ASIC regs:
        Link enable:                0x00000003
        Link err intr enable:       0x00001fff
        Link nonerr intr enable:    0x00000006
        RB config:                  0x00000001
        RB status:                  0x00000080

...
```



show contr c2c EGRESSQ_0 links all

```
RP/0/RP0/CPU0:ROUTER#sh contr c2c EGRESSQ_0 links all hw info loc 0/0/CPU0
…
    I-lite link information for link ID 0x00000e01
      Internal info:
        Bandwidth:     80 Gbps
        Status:        Up
        BP threshold:  0
        Enabled:       Datapath - Yes, Return Bus - Yes
        Flags:         0x00000000
        Debug level:   0x00000000
      ASIC regs:
        Link enable:                0x00000033
        Link err intr enable:       0x00000fff
        RB config:                  0x00000000
        RB status:                  0x00000201
        RB err intr enable:         0x000001e3
        RB nonerr intr enable:      0x0000001e

    I-lite link information for link ID 0x00010e02
      Internal info:
        Bandwidth:     80 Gbps
        Status:        Up
        BP threshold:  0
        Enabled:       Datapath - Yes, Return Bus - Yes
        Flags:         0x00000000
        Debug level:   0x00000000
      ASIC regs:
        Link enable:                0x00000033
        Link err intr enable:       0x00000fff
        RB config:                  0x00000000
        RB status:                  0x00000201
        RB err intr enable:         0x000001e3
        RB nonerr intr enable:      0x0000001e
```



show contr egressq interface …

```
RP/0/RP0/CPU0:ROUTER#sh contr egressq interface all loc 0/0/CPU0

 Interface TenGigE0/0/0/13

          Port 13
 Max LB Tokens        : 1253376
 Max LB Limit Index   : 108
 Max BS               : 312500 bytes (2500000 bits)
 Min BS               : 312500 bytes (2500000 bits)
 Quantum              : 88
 Min quantum          : 88
 Default Group        : 14
 High Priority Group  : N/A
 Low Priority Group   : 14

 Interface TenGigE0/0/0/12

          Port 12
 Max LB Tokens        : 1253376
 Max LB Limit Index   : 108
 Max BS               : 312500 bytes (2500000 bits)
 Min BS               : 312500 bytes (2500000 bits)
 Quantum              : 88
 Min quantum          : 88
 Default Group        : 13
 High Priority Group  : N/A
 Low Priority Group   : 13
```

Tokens for shaping

Bucket size

show contr egressq statistics

```
RP/0/RP0/CPU0:ROUTER#sh contr egressq statistics loc 0/0/CPU0

------------------------------------------------
              Egressq Statistics
------------------------------------------------
egressq ASIC version: 2
egressq ASIC state: Normal
plimasic link0 output packets: 16480115751827
plimasic link0 output bytes: 12708865240596442
plimasic link1 output packets: 7102320578734
plimasic link1 output bytes: 5570819605491486
cpuctrl input packets: 4408195
cpuctrl output packets: 267275838
cpuctrl output bytes: 466843951488
pse input packets: 23582699197921
egressq OOB drops: 0
cpuctrl dropped packets: 0
pse dropped packets: 0
------------------------------------------------
RP/0/RP0/CPU0:ROUTER#
```

Shortage in the packet memory (out of buffer)

Number of packets lost from the CPU

show controllers fabric link health

```
RP/0/RP0/CPU0:ROUTER(admin)#sh contr fabric link health
...
 Mismatched Plane details
 ------------------------
 Plane   Admin    Oper    up->dn          Down     Total      Down
 Id      State    State   counter         Flags    Bundles    Bundles
 ------------------------------------------------------------------

Link Usage Summary
------------------

                                        # of OPER UP Links
Rack                  Plane  Group    Min          Max        Current
Num    stage-stage     Num    Num   Required   Available   Available
-----  -----------  -----  -----  --------   ---------   ---------
0          S1-S2        0      0      N/A         N/A         N/A
0          S2-S3        0      0      N/A         N/A         N/A
0          S1-S2        0      1      N/A         N/A         N/A
0          S2-S3        0      1      N/A         N/A         N/A
0          S1-S2        1      0      N/A         N/A         N/A
0          S2-S3        1      0      N/A         N/A         N/A
0          S1-S2        1      1      N/A         N/A         N/A
0          S2-S3        1      1      N/A         N/A         N/A
0          S1-S2        2      0      N/A         N/A         N/A
0          S2-S3        2      0      N/A         N/A         N/A
0          S1-S2        2      1      N/A         N/A         N/A
0          S2-S3        2      1      N/A         N/A         N/A
0          S1-S2        3      0      N/A         N/A         N/A
0          S2-S3        3      0      N/A         N/A         N/A
...
```

16 slots chassis

N/A as expected

show controllers fabric link health

```
RP/0/RP0/CPU0:ROUTER(admin)#sh contr fabric link health
...
 Mismatched Plane details
 ------------------------
 Plane   Admin    Oper    up->dn          Down     Total      Down
 Id      State    State   counter         Flags    Bundles    Bundles
 ------------------------------------------------------------------

Link Usage Summary
------------------

                                        # of OPER UP Links
Rack                    Plane Group    Min          Max       Current
Num    stage-stage       Num   Num   Required   Available   Available
-----  -----------  -----  -----  --------   ---------   ---------
0          S1-S2        0      0      N/A         N/A         N/A
0          S2-S3        0      0      N/A         N/A         N/A
0          S1-S2        0      1      1           36          0
0          S2-S3        0      1      49          72          0
0          S1-S2        1      0      N/A         N/A         N/A
0          S2-S3        1      0      N/A         N/A         N/A
0          S1-S2        1      1      1           36          0
0          S2-S3        1      1      49          72          0
0          S1-S2        2      0      N/A         N/A         N/A
0          S2-S3        2      0      N/A         N/A         N/A
0          S1-S2        2      1      1           36          0
0          S2-S3        2      1      49          72          0
...
```

8 slots chassis

Not expected but normal

show contr fabric link port fabricqx

```
RP/0/RP0/CPU0:LYO1-CRS-1(admin)#sh contr fabric link port fabricqrx all statistics brief
Rack 0:
```

SFE R/S/M/A/P	In Data Cells	In Idle Cells	CE Cells	UCE Cells
0/0/CPU0/0/0	3846331176037	26174626745926	0	0
0/0/CPU0/0/1	2528272826683	27496664155587	0	0
0/0/CPU0/0/2	3848552507533	26176384233886	0	0
0/0/CPU0/0/3	2528272826693	27496663892227	0	0
0/0/CPU0/0/4	3846161754529	26174795835298	0	0
0/0/CPU0/0/5	2528441676265	27496494997861	0	0
0/0/CPU0/0/6	3848382428887	26176548064826	0	0
0/0/CPU0/0/7	2528441676275	27496488788634	0	0
0/0/CPU0/0/8	3846328835070	26174127215722	0	0
0/0/CPU0/0/9	2528273460430	27496161685307	0	0
0/0/CPU0/0/10	3848549456402	26175885549708	0	0
0/0/CPU0/0/11	2528273460438	27496161525907	0	0
...				
0/0/CPU0/0/26	3848360452145	26176563840192	0	0
0/0/CPU0/0/27	2528464255597	27496460017808	0	0
0/0/CPU0/0/28	3846246937967	26174698206387	0	0
0/0/CPU0/0/29	2528356431341	27496567797148	0	0
0/0/CPU0/0/30	3848467623422	26176450121411	0	0
0/0/CPU0/0/31	2528356431359	27496561283791	0	0

We'll check CE and UCE counters are not incrementing.

Fabric Troubleshooting

```
admin#show controllers fabric link health

Link Usage Summary
------------------
                                  # of OPER UP Links
Rack          Plane Group   Min       Max      Current
Num   stage-stage  Num   Num  Required  Available  Available
----- ----------- ----- ----- --------  ---------  ---------
0       S1-S2       0     0    25        36         30 (30 implies some links are down)
0       S2-S3       0     0    49        72         60 (60 implies some links are down)
0       S1-S2       0     1    25        36         36
0       S2-S3       0     1    49        72         72
0       S1-S2       1     0    25        36         36
```

```
admin#show controllers fabric plane all
 Plane  Admin   Oper      up->dn    up->mcast
 Id     State   State     counter   counter
 ------------------------------------------
 0      UP      UP        0         0
 1      UP      UP        0         0
 2      DOWN    DOWN      1         0
 3      DOWN    DOWN      1         0
 4      DOWN    DOWN      1         0
 5      DOWN    DOWN      1         0
 6      DOWN    DOWN      1         0
 7      DOWN    DOWN      1         0
```

Fabric Troubleshooting

```
admin# show controllers fabric connectivity all detail

            To Fabric  From Fabric

Card        In  Tx Planes  Rx Planes  Monitored      Total          Percent

R/S/M       Use 01234567   01234567   For (s)        Uptime (s)     Uptime

-------------------------------------------------------------------------------

0/0/CPU0    1   11111111   11111111   8115           8115           100.0000

0/1/CPU0    1   11111111   11111111   8115           8115           100.0000

0/2/CPU0    1   11.11111   11111111   8115           8115           100.0000 <- BAD

0/3/CPU0    1   11111111   11111111   8115           8115           100.0000

0/4/CPU0    1   11111111   11111111   8115           8115           100.0000
```

Fabric Troubleshooting

```
admin #show controllers fabric plane all statistics

                    In              Out          CE          UCE          PE
Plane               Cells           Cells        Cells       Cells        Cells

-------------------------------------------------------------------------------

  0        1523898476972      1523907085106       583           6           0 <-- Examine
  1      1034957920000272    1034961819119218         0           0           0
  2      1034974186949649    1034978036347613         0           0           0
  3       991530612895128     991534479449969         0           0           0
  4      1037061570260521    1037065577271822         0           0           0
  5      1034913024414752    1034916917589366         0           0           0
  6      1034873130464378    1034876921320231         0           0           0
  7      1034952869187523    1034956914144897         0           0           0
```

Q&A

Pergunta 3: Qual é a principal função de uma MSC?

(a) Dropar pacotes a nível de LPTS

(b) Processamento de pacote

(c) Captura de tráfego que é enviado a uma RP/PRP

(d) N/A

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